

MSP430FR413x Mixed-Signal Microcontrollers

1 Device Overview

1.1 Features

- Embedded Microcontroller
 - 16-Bit RISC Architecture up to 16 MHz
 - Wide Supply Voltage Range From 1.8 V to 3.6 V
- Optimized Low-Power Modes (at 3 V)
 - Active Mode: 126 μ A/MHz
 - Standby Mode: 770 nA With Real-Time Clock (RTC) Counter and Liquid Crystal Display (LCD)
 - Shutdown (LPM4.5): 15 nA
- Low-Power Ferroelectric RAM (FRAM)
 - Up to 15.5KB of Nonvolatile Memory
 - Built-In Error Correction Code (ECC)
 - Configurable Write Protection
 - Unified Memory of Program, Constants, and Storage
 - 10^{15} Write Cycle Endurance
 - Radiation Resistant and Nonmagnetic
- Intelligent Digital Peripherals
 - IR Modulation Logic
 - Two 16-Bit Timers With Three Capture/Compare Registers Each (Timer_A3)
 - One 16-Bit Counter-Only Real-Time Clock counter (RTC)
 - 16-Bit Cyclic Redundancy Checker (CRC)
- Enhanced Serial Communications
 - Enhanced USCI A (eUSCI_A) Supports UART, IrDA, and SPI
 - Enhanced USCI B (eUSCI_B) Supports SPI and I²C
- High-Performance Analog
 - 10-Channel 10-Bit Analog-to-Digital Converter (ADC)
 - Internal 1.5-V Reference
 - Sample-and-Hold 200 ksp/s
 - Low-Power Liquid Crystal Display (LCD)
 - Supports up to 4x36- or 8x32-Segment LCD Configuration
 - On-Chip Charge Pump to Keep LCD Active in Standby Mode (LPM3.5)
- Each LCD Pin Software Configurable as SEG or COM
- Contrast Control From 2.6 V to 3.5 V by 0.06-V Steps
- Clock System (CS)
 - On-Chip 32-kHz RC Oscillator (REFO)
 - On-Chip 16-MHz Digitally Controlled Oscillator (DCO) With Frequency Locked Loop (FLL)
 - $\pm 1\%$ Accuracy With On-Chip Reference at Room Temperature
 - On-Chip Very Low-Frequency 10-kHz Oscillator (VLO)
 - On-Chip High-Frequency Modulation Oscillator (MODOSC)
 - External 32-kHz Crystal Oscillator (XT1)
 - Programmable MCLK Prescaler of 1 to 128
 - SMCLK Derived From MCLK With Programmable Prescaler of 1, 2, 4, or 8
- General Input/Output and Pin Functionality
 - Total 60 I/Os on 64-Pin Package
 - 16 Interrupt Pins (P1 and P2) Can Wake Up MCU From LPMs
 - All I/Os are Capacitive Touch I/O
- Development Tools and Software
 - Free Professional Development Environments
 - Development Kit ([MSP-TS430PM64D](#))
- Family Members (Also See [Section 3](#))
 - MSP430FR4133: 15KB of Program FRAM + 512B of Information FRAM + 2KB of RAM
 - MSP430FR4132: 8KB of Program FRAM + 512B of Information FRAM + 1KB of RAM
 - MSP430FR4131: 4KB of Program FRAM + 512B of Information FRAM + 512B of RAM
- Package Options
 - 64-Pin: LQFP (PM)
 - 56-Pin: TSSOP (G56)
 - 48-Pin: TSSOP (G48)
- For Complete Module Descriptions, See the *MSP430FR4xx and MSP430FR2xx Family User's Guide* ([SLAU445](#))



1.2 Applications

- A/C Remote Controller
- Water Meter, Heat Meter, Gas Meter
- Blood Pressure Meter
- One-Time-Password Token
- Weigh Scale
- In-Building Thermostat
- Low-Power Display Driver
- Blood Glucose or Blood Pressure Meter

1.3 Description

The Texas Instruments MSP430™ family of low-power microcontrollers consists of several devices that feature different sets of peripherals targeted for various applications. The architecture, combined with extensive low-power modes, is optimized to achieve extended battery life in portable measurement applications. The device features a powerful 16-bit RISC CPU, 16-bit registers, and constant generators that contribute to maximum code efficiency. The digitally controlled oscillator (DCO) allows the device to wake up from low-power modes to active mode in less than 10 μ s.

Device Information⁽¹⁾

| PART NUMBER | PACKAGE | BODY SIZE ⁽²⁾ |
|-----------------|------------|--------------------------|
| MSP430FR4133PM | LQFP (64) | 10 mm x 10 mm |
| MSP430FR4133G56 | TSSOP (56) | 14 mm x 6.1 mm |
| MSP430FR4133G48 | TSSOP (48) | 12.5 mm x 6.1 mm |

(1) For the most current device, package, and ordering information, see the *Package Option Addendum* in [Section 9](#), or see the TI web site at www.ti.com.

(2) The sizes shown here are approximations. For the package dimensions with tolerances, see the *Mechanical Data* in [Section 9](#).

1.4 Functional Block Diagram

Figure 1-1 shows the functional block diagram.

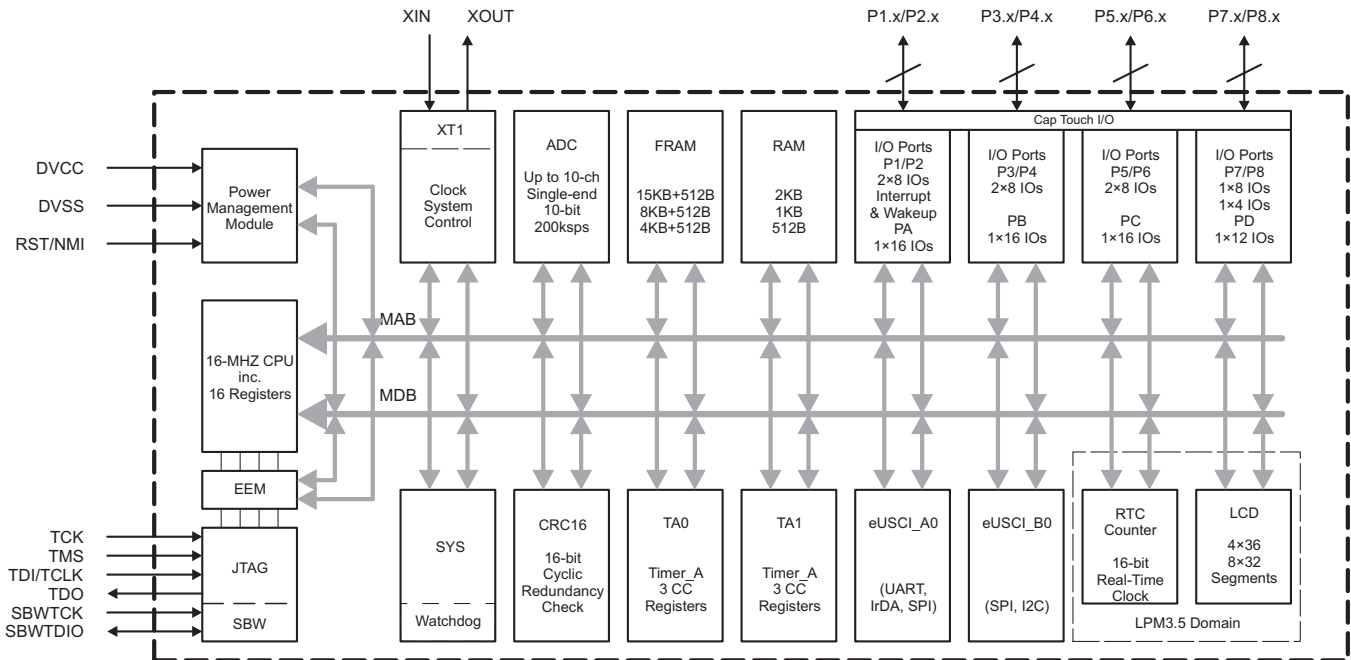


Figure 1-1. Functional Block Diagram

- The device has one main power pair of DVCC and DVSS that supplies both digital and analog modules. Recommended bypass and decouple capacitors are 4.7 μ F to 10 μ F and 0.1 μ F, respectively, with $\pm 5\%$ accuracy.
- P1 and P2 feature the pin-interrupt function and can wake the MCU from LPM3.5.
- Each Timer_A3 has three CC registers, but only the CCR1 and CCR2 are externally connected. CCR0 registers can only be used for internal period timing and interrupt generation.
- In LPM3.5, the RTC counter and the LCD can be functional while the rest of peripherals are off.
- All I/Os can be configured as Capacitive Touch I/Os.

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2 Revision History

| DATE | REVISION | NOTES |
|--------------|----------|-----------------|
| October 2014 | * | Initial Release |

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3 Device Comparison

Table 3-1 summarizes the features of the available family members.

Table 3-1. Device Comparison⁽¹⁾⁽²⁾

| DEVICE | PROGRAM FRAM + INFORMATION FRAM (BYTES) | SRAM (BYTES) | TA0, TA1 | eUSCI_A | eUSCI_B | 10-BIT ADC CHANNELS | LCD SEGMENTS | I/O | PACKAGE TYPE |
|------------------|---|-----------------|------------------------|---------|---------|------------------------|------------------|-----|---------------------|
| MSP430FR4133IPM | 15360 + 512 | 2048 | 3 × CCR ⁽³⁾ | 1 | 1 | 10 | 4 × 36 8 × 32 | 60 | 64 PM (LQFP) |
| MSP430FR4132IPM | 8192 + 512 | 1024 | 3 × CCR ⁽³⁾ | 1 | 1 | 10 | 4 × 36 8 × 32 | 60 | 64 PM (LQFP) |
| MSP430FR4131IPM | 4096 + 512 | 512 | 3 × CCR ⁽³⁾ | 1 | 1 | 10 | 4 × 36 8 × 32 | 60 | 64 PM (LQFP) |
| MSP430FR4133IG56 | 15360 + 512 | 2048 | 3 × CCR ⁽³⁾ | 1 | 1 | 8 | 4 × 30 8 × 26 | 52 | 56 DGG (TSSOP56) |
| MSP430FR4132IG56 | 8192 + 512 | 1024 | 3 × CCR ⁽³⁾ | 1 | 1 | 8 | 4 × 30 8 × 26 | 52 | 56 DGG (TSSOP56) |
| MSP430FR4131IG56 | 4096 + 512 | 512 | 3 × CCR ⁽³⁾ | 1 | 1 | 8 | 4 × 30 8 × 26 | 52 | 56 DGG (TSSOP56) |
| MSP430FR4133IG48 | 15360 + 512 | 2048 | 3 × CCR ⁽³⁾ | 1 | 1 | 8 | 4 × 24 8 × 20 | 44 | 48 DGG (TSSOP48) |
| MSP430FR4132IG48 | 8192 + 512 | 1024 | 3 × CCR ⁽³⁾ | 1 | 1 | 8 | 4 × 24 8 × 20 | 44 | 48 DGG (TSSOP48) |
| MSP430FR4131IG48 | 4096 + 512 | 512 | 3 × CCR ⁽³⁾ | 1 | 1 | 8 | 4 × 24 8 × 20 | 44 | 48 DGG (TSSOP48) |

- (1) For the most current device, package, and ordering information, see the *Package Option Addendum* in [Section 9](#), or see the TI web site at www.ti.com.
- (2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/packaging
- (3) A CCR register is a configurable register that provides internal and external capture or compare inputs, or internal and external PWM outputs.

4 Terminal Configuration and Functions

4.1 Pin Diagrams

Figure 4-1 shows the 64-pin PM package.

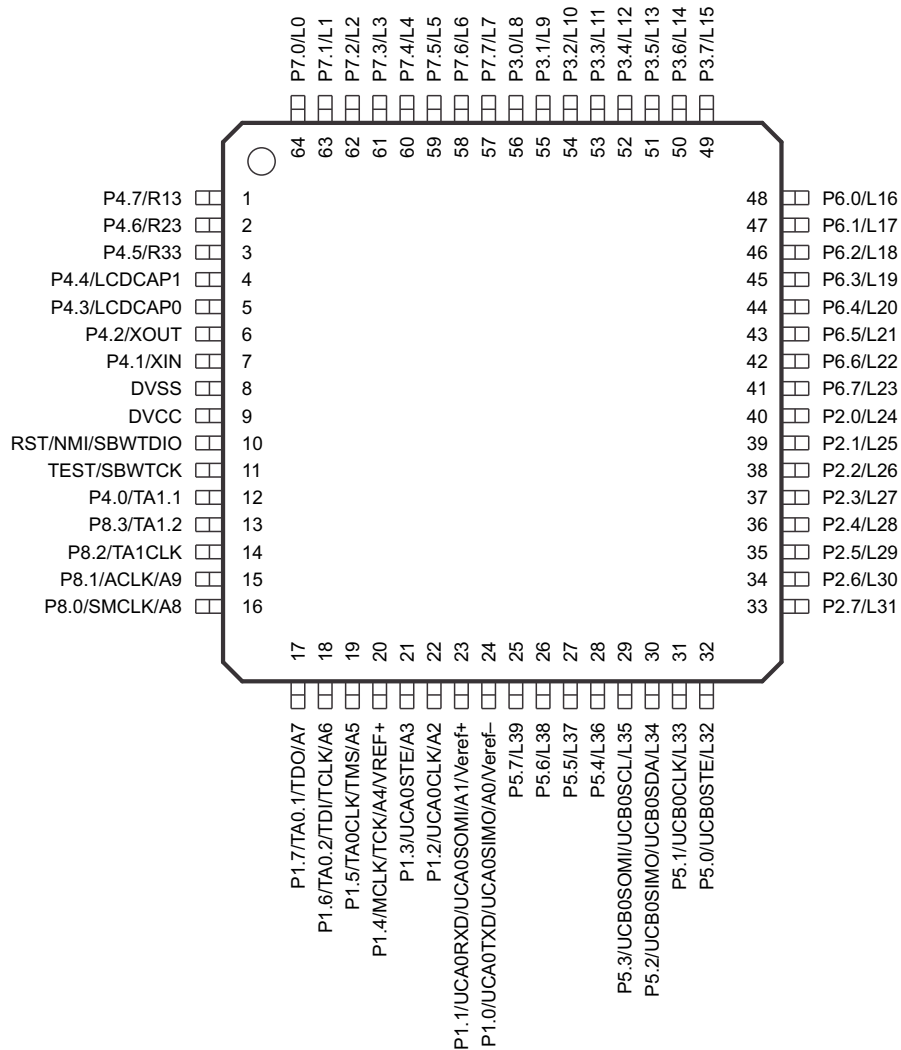


Figure 4-1. 64-Pin PM (LQFP) (Top View)

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Figure 4-2 shows the 56-pin DGG package.

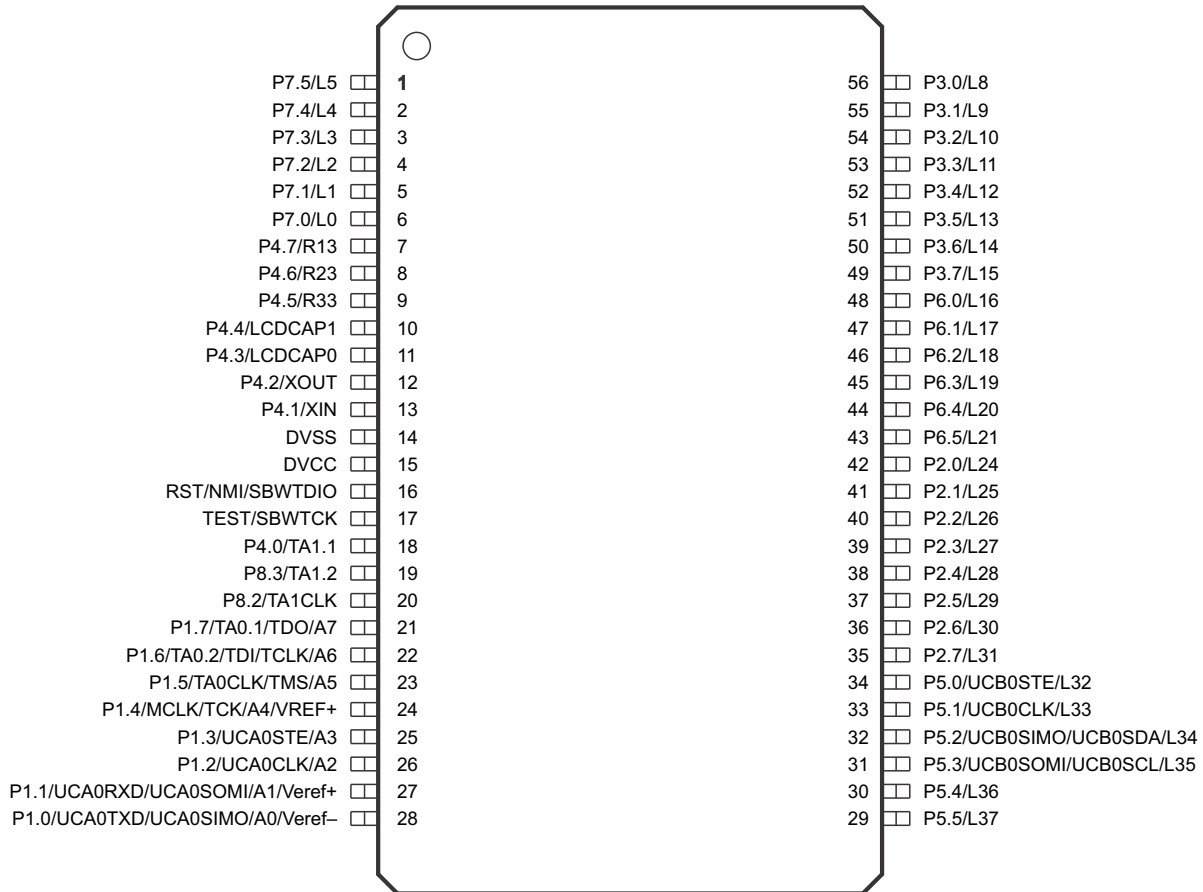


Figure 4-2. 56-Pin DGG (TSSOP) (Top View)

Figure 4-3 shows the 48-pin DGG package.

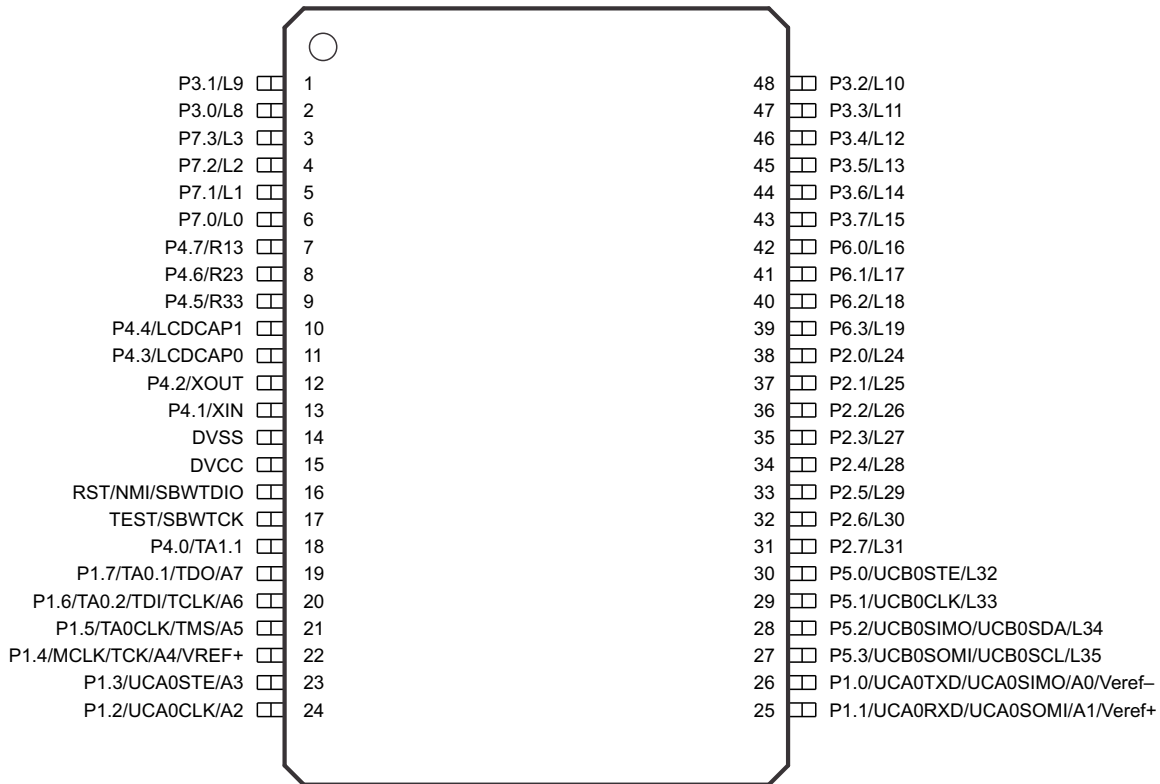


Figure 4-3. 48-Pin DGG (TSSOP) Designation

4.2 Signal Descriptions

Table 4-1 describes the signals for all device variants and package options.

Table 4-1. Signal Descriptions

| TERMINAL | | | | I/O | DESCRIPTION |
|---|----------------|-----|-----|-----|--|
| NAME | PACKAGE SUFFIX | | | | |
| | PM | G56 | G48 | | |
| P4.7/R13 | 1 | 7 | 7 | I/O | General-purpose I/O Input/output port of third most positive analog LCD voltage V4 |
| P4.6/R23 | 2 | 8 | 8 | I/O | General-purpose I/O Input/output port of second most positive analog LCD voltage V2 |
| P4.5/R33 | 3 | 9 | 9 | I/O | General-purpose I/O Input/output port of first most positive analog LCD voltage V1 |
| P4.4/LCDCAP1 | 4 | 10 | 10 | I/O | General-purpose I/O LCD charge pump external port connecting to LCDCAP0 pin by 0.1- μ F capacitor |
| P4.3/LCDCAP0 | 5 | 11 | 11 | I/O | General-purpose I/O LCD charge pump external port connecting to LCDCAP1 pin by 0.1- μ F capacitor |
| P4.2/XOUT | 6 | 12 | 12 | I/O | General-purpose I/O Output terminal for crystal oscillator |
| P4.1/XIN | 7 | 13 | 13 | I/O | General-purpose I/O Input terminal for crystal oscillator |
| DVSS | 8 | 14 | 14 | | Power ground |
| DVCC | 9 | 15 | 15 | | Power supply |
| $\overline{\text{RST}}/\text{NMI}/\text{SBWTDIO}$ | 10 | 16 | 16 | I/O | Reset input active low Non-maskable interrupt input Spy-Bi-Wire data input/output |
| TEST/SBWTK | 11 | 17 | 17 | I | Test Mode pin – selected digital I/O on JTAG pins Spy-Bi-Wire input clock |
| P4.0/TA1.1 | 12 | 18 | 18 | I/O | General-purpose I/O Timer TA1 CCR1 capture: CCI1A input, compare: Out1 outputs |
| P8.3/TA1.2 ⁽¹⁾ | 13 | 19 | | I/O | General-purpose I/O Timer TA1 CCR2 capture: CCI2A input, compare: Out2 outputs |
| P8.2/TA1CLK ⁽¹⁾ | 14 | 20 | | I/O | General-purpose I/O Timer clock input TACLK for TA1 |
| P8.1/ACLK/A9 ⁽¹⁾ | 15 | | | I/O | General-purpose I/O ACLK output Analog input A9 |
| P8.0/SMCLK/A8 ⁽¹⁾ | 16 | | | I/O | General-purpose I/O SMCLK output Analog input A8 |
| P1.7/TA0.1/TDO/A7 | 17 | 21 | 19 | I/O | General-purpose I/O ⁽²⁾ Timer TA0 CCR1 capture: CCI1A input, compare: Out1 outputs Test data output Analog input A7 |
| P1.6/TA0.2/TDI/TCLK/A6 | 18 | 22 | 20 | I/O | General-purpose I/O ⁽²⁾ Timer TA0 CCR2 capture: CCI2A input, compare: Out2 outputs Test data input or test clock input Analog input A6 |
| P1.5/TA0CLK/TMS/A5 | 19 | 23 | 21 | I/O | General-purpose I/O ⁽²⁾ Timer clock input TACLK for TA0 Test mode select Analog input A5 |

- (1) Any pin that is not bonded out in a smaller package must be initialized by software after reset to achieve the lowest leakage current.
(2) Because this pin is multiplexed with the JTAG function, it is recommended to disable the pin interrupt function while in JTAG debug to prevent collisions.

Table 4-1. Signal Descriptions (continued)

| TERMINAL | | | | I/O | DESCRIPTION |
|------------------------------------|----------------|-----|-----|-----|---|
| NAME | PACKAGE SUFFIX | | | | |
| | PM | G56 | G48 | | |
| P1.4/MCLK/TCK/A4/VREF+ | 20 | 24 | 22 | I/O | General-purpose I/O ⁽²⁾ MCLK output Test clock Analog input A4 Output of positive reference voltage with ground as reference |
| P1.3/UCA0STE/A3 | 21 | 25 | 23 | I/O | General-purpose I/O eUSCI_A0 SPI slave transmit enable Analog input A3 |
| P1.2/UCA0CLK/A2 | 22 | 26 | 24 | I/O | General-purpose I/O eUSCI_A0 SPI clock input/output Analog input A2 |
| P1.1/UCA0RXD/UCA0SOMI/ A1/Vref+ | 23 | 27 | 25 | I/O | General-purpose I/O eUSCI_A0 UART receive data eUSCI_A0 SPI slave out/master in Analog input A1, and ADC positive reference |
| P1.0/UCA0TXD/UCA0SIMO/ A0/Vref- | 24 | 28 | 26 | I/O | General-purpose I/O eUSCI_A0 UART transmit data eUSCI_A0 SPI slave in/master out Analog input A0, and ADC negative reference |
| P5.7/L39 ⁽¹⁾ | 25 | | | I/O | General-purpose I/O LCD drive pin; either segment or common output |
| P5.6/L38 ⁽³⁾ | 26 | | | I/O | General-purpose I/O LCD drive pin; either segment or common output |
| P5.5/L37 ⁽³⁾ | 27 | 29 | | I/O | General-purpose I/O LCD drive pin; either segment or common output |
| P5.4/L36 ⁽³⁾ | 28 | 30 | | I/O | General-purpose I/O LCD drive pin; either segment or common output |
| P5.3/UCB0SOMI/UCB0SCL/L35 | 29 | 31 | 27 | I/O | General-purpose I/O eUSCI_B0 SPI slave out/master in; eUSCI_B0 I2C clock LCD drive pin; either segment or common output |
| P5.2/UCB0SIMO/UCB0SDA/L34 | 30 | 32 | 28 | I/O | General-purpose I/O eUSCI_B0 SPI slave in/master out; eUSCI_B0 I2C data LCD drive pin; either segment or common output |
| P5.1/UCB0CLK/L33 | 31 | 33 | 29 | I/O | General-purpose I/O eUSCI_B0 clock input/output LCD drive pin; either segment or common output |
| P5.0/UCB0STE/L32 | 32 | 34 | 30 | I/O | General-purpose I/O eUSCI_B0 slave transmit enable LCD drive pin; either segment or common output |
| P2.7/L31 | 33 | 35 | 31 | I/O | General-purpose I/O LCD drive pin; either segment or common output |
| P2.6/L30 | 34 | 36 | 32 | I/O | General-purpose I/O LCD drive pin; either segment or common output |
| P2.5/L29 | 35 | 37 | 33 | I/O | General-purpose I/O LCD drive pin; either segment or common output |
| P2.4/L28 | 36 | 38 | 34 | I/O | General-purpose I/O LCD drive pin; either segment or common output |
| P2.3/L27 | 37 | 39 | 35 | I/O | General-purpose I/O LCD drive pin; either segment or common output |
| P2.2/L26 | 38 | 40 | 36 | I/O | General-purpose I/O LCD drive pin; either segment or common output |
| P2.1/L25 | 39 | 41 | 37 | I/O | General-purpose I/O LCD drive pin; either segment or common output |
| P2.0/L24 | 40 | 42 | 38 | I/O | General-purpose I/O LCD drive pin; either segment or common output |

(3) Any pin that is not bonded out in a smaller package must be initialized by software after reset to achieve the lowest leakage current.

Table 4-1. Signal Descriptions (continued)

| TERMINAL | | | | I/O | DESCRIPTION |
|-------------------------|----------------|-----|-----|-----|---|
| NAME | PACKAGE SUFFIX | | | | |
| | PM | G56 | G48 | | |
| P6.7/L23 ⁽³⁾ | 41 | | | I/O | General-purpose I/O LCD drive pin; either segment or common output |
| P6.6/L22 ⁽³⁾ | 42 | | | I/O | General-purpose I/O LCD drive pin; either segment or common output |
| P6.5/L21 ⁽³⁾ | 43 | 43 | | I/O | General-purpose I/O LCD drive pin; either segment or common output |
| P6.4/L20 ⁽³⁾ | 44 | 44 | | I/O | General-purpose I/O LCD drive pin; either segment or common output |
| P6.3/L19 | 45 | 45 | 39 | I/O | General-purpose I/O LCD drive pin; either segment or common output |
| P6.2/L18 | 46 | 46 | 40 | I/O | General-purpose I/O LCD drive pin; either segment or common output |
| P6.1/L17 | 47 | 47 | 41 | I/O | General-purpose I/O LCD drive pin; either segment or common output |
| P6.0/L16 | 48 | 48 | 42 | I/O | General-purpose I/O LCD drive pin; either segment or common output |
| P3.7/L15 | 49 | 49 | 43 | I/O | General-purpose I/O LCD drive pin; either segment or common output |
| P3.6/L14 | 50 | 50 | 44 | I/O | General-purpose I/O LCD drive pin; either segment or common output |
| P3.5/L13 | 51 | 51 | 45 | I/O | General-purpose I/O LCD drive pin; either segment or common output |
| P3.4/L12 | 52 | 52 | 46 | I/O | General-purpose I/O LCD drive pin; either segment or common output |
| P3.3/L11 | 53 | 53 | 47 | I/O | General-purpose I/O LCD drive pin; either segment or common output |
| P3.2/L10 | 54 | 54 | 48 | I/O | General-purpose I/O LCD drive pin; either segment or common output |
| P3.1/L9 | 55 | 55 | 1 | I/O | General-purpose I/O LCD drive pin; either segment or common output |
| P3.0/L8 | 56 | 56 | 2 | I/O | General-purpose I/O LCD drive pin; either segment or common output |
| P7.7/L7 ⁽⁴⁾ | 57 | | | I/O | General-purpose I/O LCD drive pin; either segment or common output |
| P7.6/L6 ⁽⁴⁾ | 58 | | | I/O | General-purpose I/O LCD drive pin; either segment or common output |
| P7.5/L5 ⁽⁴⁾ | 59 | 1 | | I/O | General-purpose I/O LCD drive pin; either segment or common output |
| P7.4/L4 ⁽⁴⁾ | 60 | 2 | | I/O | General-purpose I/O LCD drive pin; either segment or common output |
| P7.3/L3 | 61 | 3 | 3 | I/O | General-purpose I/O LCD drive pin; either segment or common output |
| P7.2/L2 | 62 | 4 | 4 | I/O | General-purpose I/O LCD drive pin; either segment or common output |
| P7.1/L1 | 63 | 5 | 5 | I/O | General-purpose I/O LCD drive pin; either segment or common output |
| P7.0/L0 | 64 | 6 | 6 | I/O | General-purpose I/O LCD drive pin; either segment or common output |

(4) Any pin that is not bonded out in a smaller package must be initialized by software after reset to achieve the lowest leakage current.

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4.3 Pin Multiplexing

Pin multiplexing for these devices is controlled by both register settings and operating modes (for example, if the device is in test mode). For details of the settings for each pin and schematics of the multiplexed ports, see [Section 6.9.13](#).

4.4 Connection of Unused Pins

[Table 4-2](#) shows the correct termination of unused pins.

Table 4-2. Connection of Unused Pins⁽¹⁾

| PIN | POTENTIAL | COMMENT |
|------------------------------------|-----------|--|
| Px.0 to Px.7 | Open | Switched to port function, output direction (PxDIR.n = 1) |
| $\overline{\text{RST}}/\text{NMI}$ | DVCC | 47-k Ω pullup or internal pullup selected with 10-nF (1.1 nF) pulldown ⁽²⁾ |
| TEST | Open | This pin always has an internal pulldown enabled. |

- (1) Any unused pin with a secondary function that is shared with general-purpose I/O should follow the Px.0 to Px.7 unused pin connection guidelines.
- (2) The pulldown capacitor should not exceed 1.1 nF when using devices with Spy-Bi-Wire interface in Spy-Bi-Wire mode with TI tools like FET interfaces or GANG programmers.

5 Specifications

5.1 Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | MIN | MAX | UNIT |
|--|------|------------------------------------|------|
| Voltage applied at DVCC pin to V _{SS} | -0.3 | 4.1 | V |
| Voltage applied to any pin ⁽²⁾ | -0.3 | V _{CC} + 0.3 (4.1 Max) | V |
| Diode current at any device pin | | ±2 | mA |
| Maximum junction temperature, T _J | | 85 | °C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages referenced to V_{SS}.

5.2 Handling Ratings

| | MIN | MAX | UNIT |
|--|-----|-----|------|
| T _{stg} Storage temperature range | -40 | 125 | °C |

5.3 Recommended Operating Conditions

Typical values are specified at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted)

| | MIN | NOM | MAX | UNIT |
|--|---|-----|-------------------|------|
| V _{CC} Supply voltage applied at DVCC pin ⁽¹⁾⁽²⁾⁽³⁾ | 1.8 | | 3.6 | V |
| V _{SS} Supply voltage applied at DVSS pin | | 0 | | V |
| T _A Operating free-air temperature | -40 | | 85 | °C |
| T _J Operating junction temperature | -40 | | 85 | °C |
| C _{DVCC} Recommended capacitor at DVCC ⁽⁴⁾ | 4.7 | 10 | | µF |
| f _{SYSTEM} Processor frequency (maximum MCLK frequency) ⁽³⁾⁽⁵⁾ | No FRAM wait states (NWAITSx = 0) | 0 | 8 | MHz |
| | With FRAM wait states (NWAITSx = 1) ⁽⁶⁾ | 0 | 16 ⁽⁷⁾ | |
| f _{ACLK} Maximum ACLK frequency | | | 40 | kHz |
| f _{SMCLK} Maximum SMCLK frequency | | | 16 ⁽⁷⁾ | MHz |

- (1) Supply voltage changes faster than 0.2 V/µs can trigger a BOR reset even within the recommended supply voltage range.
- (2) Modules may have a different supply voltage range specification. See the specification of the respective module in this data sheet.
- (3) The minimum supply voltage is defined by the SVS levels. Refer to the SVS threshold parameters in [Table 5-1](#).
- (4) A capacitor tolerance of ±20% or better is required.
- (5) Modules may have a different maximum input clock specification. See the specification of the respective module in this data sheet.
- (6) Wait states only occur on actual FRAM accesses (that is, on FRAM cache misses). RAM and peripheral accesses are always executed without wait states.
- (7) If clock sources such as HF crystals or the DCO with frequencies >16 MHz are used, the clock must be divided in the clock system to comply with this operating condition.

5.4 Active Mode Supply Current Into V_{CC} Excluding External Current

 See ⁽¹⁾

| PARAMETER | EXECUTION MEMORY | TEST CONDITIONS | Frequency ($f_{MCLK} = f_{SMCLK}$) | | | | | | UNIT |
|-----------------------|------------------------------|-----------------|---|-----|---|-----|---|------|---------|
| | | | 1 MHz 0 WAIT STATES (NWAITSx = 0) | | 8 MHz 0 WAIT STATES (NWAITSx = 0) | | 16 MHz 1 WAIT STATE (NWAITSx = 1) | | |
| | | | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{AM, FRAM(0\%)}$ | FRAM 0% cache hit ratio | 3 V, 25°C | 504 | | 2874 | | 3156 | 3700 | μA |
| | | 3 V, 85°C | 516 | | 2919 | | 3205 | | μA |
| $I_{AM, FRAM(100\%)}$ | FRAM 100% cache hit ratio | 3 V, 25°C | 209 | | 633 | | 1056 | 1298 | μA |
| | | 3 V, 85°C | 217 | | 647 | | 1074 | | μA |
| $I_{AM, RAM}^{(2)}$ | RAM | 3 V, 25°C | 231 | | 809 | | 1450 | | μA |

(1) All inputs are tied to 0 V or to V_{CC} . Outputs do not source or sink any current. Characterized with program executing typical data processing.

$f_{ACLK} = 32786$ Hz, $f_{MCLK} = f_{SMCLK} = f_{DCO}$ at specified frequency

Program and data entirely reside in FRAM. All execution is from FRAM.

(2) Program and data reside entirely in RAM. All execution is from RAM. No access to FRAM.

5.5 Active Mode Supply Current Per MHz

 $V_{CC} = 3$ V, $T_A = 25^\circ C$ (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | TYP | UNIT |
|-------------------|---|-----|-------------|
| $dI_{AM,FRAM}/df$ | Active mode current consumption per MHz, execution from FRAM, no wait states ⁽¹⁾ | 126 | $\mu A/MHz$ |

$((I_{AM, 75\% \text{ cache hit rate at } 8 \text{ MHz}}) - (I_{AM, 75\% \text{ cache hit rate at } 1 \text{ MHz}})) / 7 \text{ MHz}$

(1) All peripherals are turned on in default settings.

5.6 Low-Power Mode LPM0 Supply Currents Into V_{CC} Excluding External Current

 $V_{CC} = 3$ V, $T_A = 25^\circ C$ (unless otherwise noted)⁽¹⁾⁽²⁾

| PARAMETER | V_{CC} | FREQUENCY (f_{SMCLK}) | | | | | | UNIT |
|---|----------|---------------------------|-----|-------|-----|--------|-----|---------|
| | | 1 MHz | | 8 MHz | | 16 MHz | | |
| | | TYP | MAX | TYP | MAX | TYP | MAX | |
| I_{LPM0} Low-power mode LPM0 supply current | 2 V | 158 | | 307 | | 415 | | μA |
| | 3 V | 169 | | 318 | | 427 | | |

(1) All inputs are tied to 0 V or to V_{CC} . Outputs do not source or sink any current.

(2) Current for watchdog timer clocked by SMCLK included.

$f_{ACLK} = 32786$ Hz, $f_{MCLK} = 0$ MHz, f_{SMCLK} at specified frequency.

5.7 Low-Power Mode LPM3, LPM4 Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) ⁽¹⁾

| PARAMETER | V_{CC} | -40°C | | 25°C | | 85°C | | UNIT |
|--|----------|-------|-----|------|------|------|-----|---------|
| | | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{LPM3,XT1}$ Low-power mode 3, includes SVS ⁽²⁾⁽³⁾⁽⁴⁾ | 3 V | 1.13 | | 1.31 | 1.99 | 3.00 | | μA |
| | 2 V | 1.06 | | 1.21 | | 2.94 | | |
| $I_{LPM3,VLO}$ Low-power mode 3, VLO, excludes SVS ⁽⁵⁾ | 3 V | 0.92 | | 1.00 | 1.75 | 2.89 | | μA |
| | 2 V | 0.86 | | 1.00 | | 2.75 | | |
| $I_{LPM3,LCD,CP}$ Low-power mode 3, LCD, excludes SVS ⁽⁶⁾ | 3 V | 1.07 | | 1.25 | | 3.04 | | μA |
| $I_{LPM3,RTC}$ Low-power mode 3, RTC, excludes SVS ⁽⁷⁾ | 3 V | 1.08 | | 1.25 | | 3.04 | | μA |
| $I_{LPM4,SVS}$ Low-power mode 4, includes SVS | 3 V | 0.65 | | 0.75 | | 1.88 | | μA |
| | 2 V | 0.63 | | 0.73 | | 1.85 | | |
| I_{LPM4} Low-power mode 4, excludes SVS | 3 V | 0.51 | | 0.58 | | 1.51 | | μA |
| | 2 V | 0.50 | | 0.57 | | 1.49 | | |

(1) All inputs are tied to 0 V or to V_{CC} . Outputs do not source or sink any current

(2) Not applicable for devices with HF crystal oscillator only.

(3) Characterized with a Golledge MS1V-TK/I_32.768KHZ crystal with a load capacitance chosen to closely match the required load.

(4) **Low-power mode 3, includes SVS** test conditions:

Current for watchdog timer clocked by ACLK and RTC clocked by XT1 included. Current for brownout and SVS included (SVSHE = 1). CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 0 (LPM3), $f_{XT1} = 32768$ Hz, $f_{ACLK} = f_{XT1}$, $f_{MCLK} = f_{SMCLK} = 0$ MHz

(5) **Low-power mode 3, VLO, excludes SVS** test conditions:

Current for watchdog timer clocked by VLO included. RTC disabled. Current for brownout included. SVS disabled (SVSHE = 0). CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 0 (LPM3), $f_{XT1} = 0$ Hz, $f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0$ MHz

(6) LCD works in LPM3 if internal charge pump and V_{REF} switch mode are enabled. LCD driver pins are configured as 4 × 36 at 32-Hz frame frequency with external 32768-Hz clock source.

(7) RTC periodically wakes up every second with external 32768-Hz as source.

5.8 Low-Power Mode LPMx.5 Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | V_{CC} | -40°C | | 25°C | | 85°C | | UNIT |
|-----------------------|--|----------|-------|-----|-------|-------|-------|-------|---------|
| | | | TYP | MAX | TYP | MAX | TYP | MAX | |
| $I_{LPM3.5, XT1}$ | Low-power mode 3.5, includes SVS ⁽¹⁾⁽²⁾⁽³⁾ (also refer to Figure 5-3) | 3 V | 0.71 | | 0.77 | 1.25 | 1.06 | 2.06 | μA |
| | | 2 V | 0.66 | | 0.70 | | 0.95 | | |
| $I_{LPM3.5, LCD, CP}$ | Low-power mode 3.5, excludes SVS ⁽⁴⁾ | 3 V | | | 0.94 | | | | μA |
| $I_{LPM4.5, SVS}$ | Low-power mode 4.5, includes SVS ⁽⁵⁾ | 3 V | 0.23 | | 0.25 | 0.375 | 0.32 | 0.43 | μA |
| | | 2 V | 0.20 | | 0.20 | | 0.24 | | |
| $I_{LPM4.5}$ | Low-power mode 4.5, excludes SVS ⁽⁶⁾ | 3 V | 0.010 | | 0.015 | 0.070 | 0.073 | 0.140 | μA |
| | | 2 V | 0.008 | | 0.013 | | 0.060 | | |

(1) Not applicable for devices with HF crystal oscillator only.

(2) Characterized with a Micro Crystal MS1V-T1K crystal with a load capacitance chosen to closely match the required load.

(3) **Low-power mode 3.5, includes SVS** test conditions:

Current for RTC clocked by XT1 included. Current for brownout and SVS included (SVSHE = 1). Core regulator disabled.

PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),

$f_{XT1} = 32768$ Hz, $f_{ACLK} = f_{XT1}$, $f_{MCLK} = f_{SMCLK} = 0$ MHz

(4) LCD works in LPM3.5 if the internal charge pump and VREF switch mode are enabled. The LCD driver pins are configured as 4x36 at 32-Hz frame frequency with an external 32768-Hz clock source.

(5) **Low-power mode 4.5, includes SVS** test conditions:

Current for brownout and SVS included (SVSHE = 1). Core regulator disabled.

PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),

$f_{XT1} = 0$ Hz, $f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0$ MHz

(6) **Low-power mode 4.5, excludes SVS** test conditions:

Current for brownout included. SVS disabled (SVSHE = 0). Core regulator disabled.

PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),

$f_{XT1} = 0$ Hz, $f_{ACLK} = f_{MCLK} = f_{SMCLK} = 0$ MHz

5.9 Typical Characteristics, Low-Power Mode Supply Currents

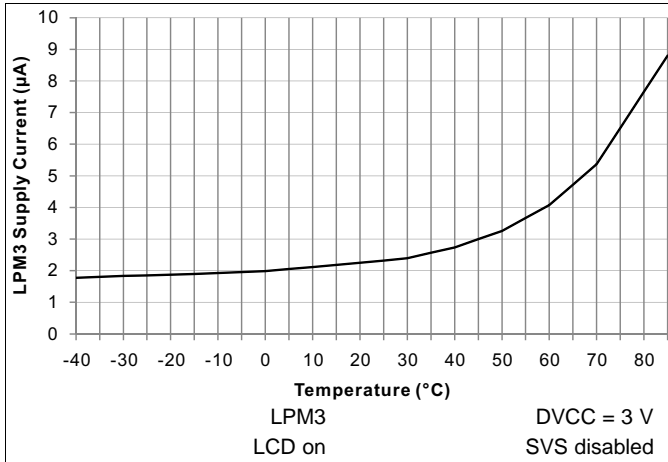


Figure 5-1. LPM3 Supply Current vs Temperature

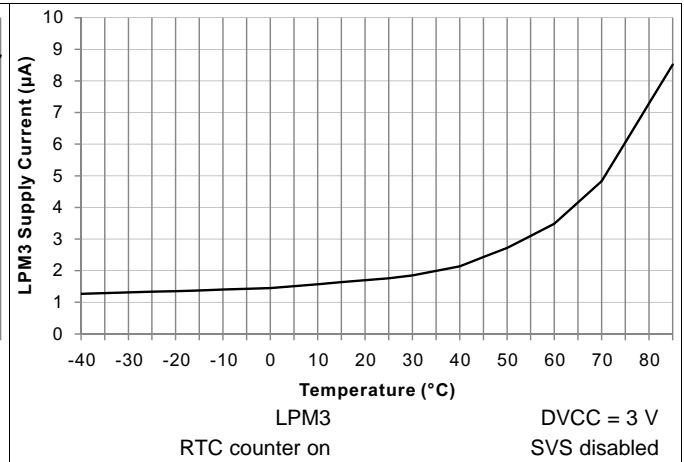


Figure 5-2. LPM3 Supply Current vs Temperature

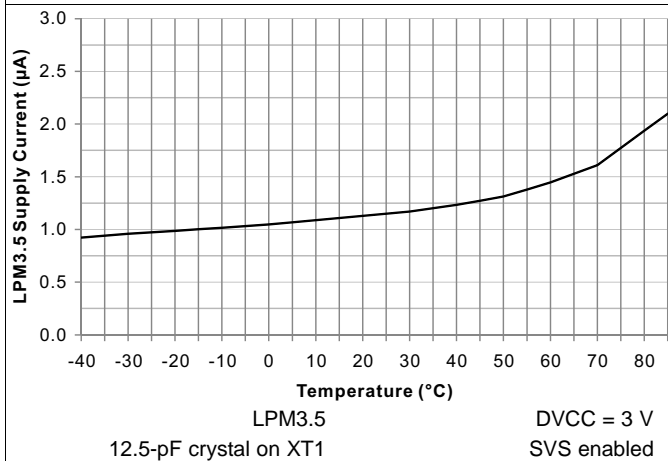


Figure 5-3. LPM3.5 Supply Current vs Temperature

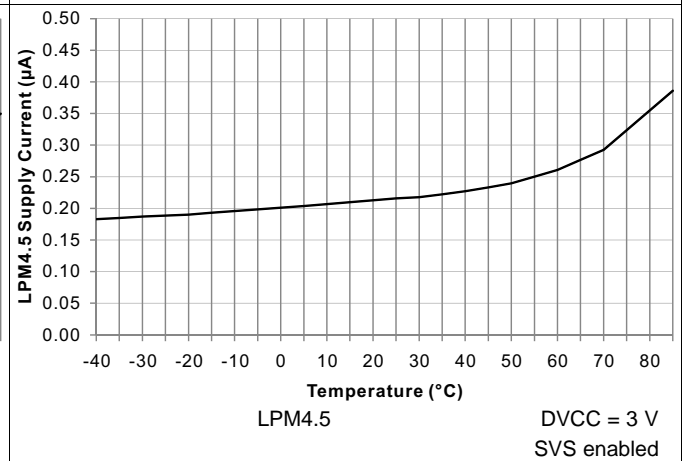


Figure 5-4. LPM4.5 Supply Current vs Temperature

PRODUCT PREVIEW

5.10 Typical Characteristics - Current Consumption Per Module

| MODULE | TEST CONDITIONS | REFERENCE CLOCK | TYP | UNIT |
|---------|----------------------------------|--------------------|-----|--------|
| Timer_A | | Module input clock | 5 | μA/MHz |
| eUSCI_A | UART mode | Module input clock | 7 | μA/MHz |
| eUSCI_A | SPI mode | Module input clock | 5 | μA/MHz |
| eUSCI_B | SPI mode | Module input clock | 5 | μA/MHz |
| eUSCI_B | I ² C mode, 100 kbaud | Module input clock | 5 | μA/MHz |
| RTC | | 32 kHz | 85 | nA |
| CRC | From start to end of operation | MCLK | 8.5 | μA/MHz |

5.11 Thermal Packaging Characteristics

| PARAMETERS | | VALUE | UNIT |
|----------------------|--|------------------|------|
| θ_{JA} | Junction-to-ambient thermal resistance, still air ⁽¹⁾ | 61.7 | °C/W |
| $\theta_{JC, (TOP)}$ | Junction-to-case (top) thermal resistance ⁽²⁾ | 25.4 | °C/W |
| θ_{JB} | Junction-to-board thermal resistance ⁽³⁾ | 32.7 | °C/W |
| Ψ_{JB} | Junction-to-board thermal characterization parameter | 32.4 | °C/W |
| Ψ_{JT} | Junction-to-top thermal characterization parameter | 2.5 | °C/W |
| | | LQFP-64 (PM) | |
| θ_{JA} | Junction-to-ambient thermal resistance, still air ⁽¹⁾ | 62.4 | °C/W |
| $\theta_{JC, (TOP)}$ | Junction-to-case (top) thermal resistance ⁽²⁾ | 18.7 | °C/W |
| θ_{JB} | Junction-to-board thermal resistance ⁽³⁾ | 31.4 | °C/W |
| Ψ_{JB} | Junction-to-board thermal characterization parameter | 31.1 | °C/W |
| Ψ_{JT} | Junction-to-top thermal characterization parameter | 0.8 | °C/W |
| | | TSSOP-56 (DGG56) | |
| θ_{JA} | Junction-to-ambient thermal resistance, still air ⁽¹⁾ | 68.9 | °C/W |
| $\theta_{JC, (TOP)}$ | Junction-to-case (top) thermal resistance ⁽²⁾ | 23 | °C/W |
| θ_{JB} | Junction-to-board thermal resistance ⁽³⁾ | 35.8 | °C/W |
| Ψ_{JB} | Junction-to-board thermal characterization parameter | 35.3 | °C/W |
| Ψ_{JT} | Junction-to-top thermal characterization parameter | 1.1 | °C/W |
| | | TSSOP-48 (DGG48) | |

- (1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, High-K board, as specified in JESD51-7, in an environment described in JESD51-2a.
- (2) The junction-to-case (top) thermal resistance is obtained by simulating a cold place test on the package top. No specific JEDEC-standard test exists, but a close description can be found in the ANSI SEMI standard G30-88.
- (3) The junction-to-board thermal resistance is obtained by simulating in an environment with a ring cold place fixture to control the PCB temperature, as described in JESD51-8.

5.12 Timing and Switching Characteristics

5.12.1 Power Supply Sequencing

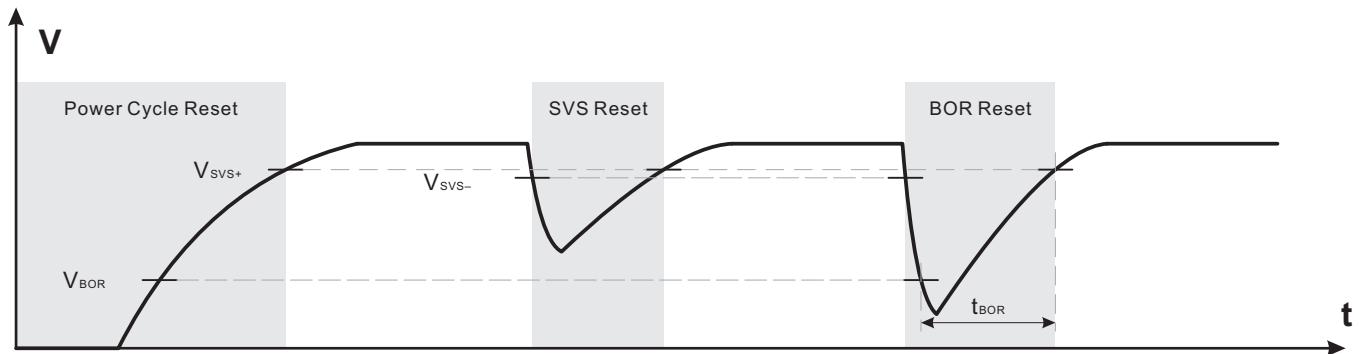


Figure 5-5. Power Cycle, SVS, and BOR Reset Conditions

Table 5-1. PMM, SVS and BOR

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---------------------|---|------------------|------|------|------|---------|
| $V_{BOR, safe}$ | Safe BOR power-down level ⁽¹⁾ | | 0.1 | | | V |
| $t_{BOR, safe}$ | Safe BOR reset delay ⁽²⁾ | | 10 | | | ms |
| $I_{SVSH, AM}$ | SVS _H current consumption, active mode | $V_{CC} = 3.6 V$ | | | 1.5 | μA |
| $I_{SVSH, LPM}$ | SVS _H current consumption, low-power modes | $V_{CC} = 3.6 V$ | | 240 | | nA |
| V_{SVSH-} | SVS _H power-down level | | 1.71 | 1.81 | 1.87 | V |
| V_{SVSH+} | SVS _H power-up level | | 1.76 | 1.88 | 1.99 | V |
| $V_{SVSH, hys}$ | SVS _H hysteresis | | | 70 | | mV |
| $t_{PD, SVSH, AM}$ | SVS _H propagation delay, active mode | | | | 10 | μs |
| $t_{PD, SVSH, LPM}$ | SVS _H propagation delay, low-power modes | | | | 100 | μs |

(1) A safe BOR can be correctly generated only if DVCC drops below this voltage before it rises.

(2) When an BOR occurs, a safe BOR can be correctly generated only if DVCC is kept low longer than this period before it reaches V_{SVSH+} .

5.12.2 Reset Timing

Table 5-2. Wake-Up Times From Low-Power Modes and Reset

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------------------|---|-----------------|-----------------|-----|-----|-------------------------------|------|
| t _{WAKE-UP FRAM} | Additional wake-up time to activate the FRAM in AM if previously disabled by the FRAM controller or from a LPM if immediate activation is selected for wake-up ⁽¹⁾ | | 3 V | | 10 | | μs |
| t _{WAKE-UP LPM0} | Wake-up time from LPM0 to active mode ⁽¹⁾ | | 3 V | | | 200 ns + 2.5/t _{DCO} | |
| t _{WAKE-UP LPM3} | Wake-up time from LPM3 to active mode ⁽²⁾ | | 3 V | | 10 | | μs |
| t _{WAKE-UP LPM4} | Wake-up time from LPM4 to active mode | | 3 V | | 10 | | μs |
| t _{WAKE-UP LPM3.5} | Wake-up time from LPM3.5 to active mode ⁽²⁾ | | 3 V | | 350 | | μs |
| t _{WAKE-UP LPM4.5} | Wake-up time from LPM4.5 to active mode ⁽²⁾ | SVSHE = 1 | 3 V | | 350 | | μs |
| | | SVSHE = 0 | 3 V | | 1 | | ms |
| t _{WAKE-UP-RESET} | Wake-up time from $\overline{\text{RST}}$ or BOR event to active mode ⁽²⁾ | | 3 V | | 1 | | ms |
| t _{RESET} | Pulse duration required at $\overline{\text{RST}}$ /NMI pin to accept a reset | | 3 V | 2 | | | μs |

- (1) The wake-up time is measured from the edge of an external wake-up signal (for example, port interrupt or wake-up event) to the first externally observable MCLK clock edge.
- (2) The wake-up time is measured from the edge of an external wake-up signal (for example, port interrupt or wake-up event) until the first instruction of the user program is executed.

5.12.3 Clock Specifications

Table 5-3. XT1 Crystal Oscillator (Low Frequency)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (See note ⁽¹⁾)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|--------------------------|--|--|-----------------|-----|-------|------|------|
| f _{XT1, LF} | XT1 oscillator crystal, low frequency | LFXTBYPASS = 0 | | | 32768 | | Hz |
| DC _{XT1, LF} | XT1 oscillator LF duty cycle | Measured at MCLK, f _{LFXT} = 32768 Hz | | 30% | | 70% | |
| f _{XT1, SW} | XT1 oscillator logic-level square-wave input frequency | LFXTBYPASS = 1 ⁽²⁾⁽³⁾ | | | 32768 | | Hz |
| DC _{XT1, SW} | LFXT oscillator logic-level square-wave input duty cycle | LFXTBYPASS = 1 | | 40% | | 60% | |
| OA _{LFXT} | Oscillation allowance for LF crystals ⁽⁴⁾ | LFXTBYPASS = 0, LFXTDRIVE = {3}, f _{LFXT} = 32768 Hz, C _{L,eff} = 12.5 pF | | | 200 | | kΩ |
| C _{L,eff} | Integrated effective load capacitance ⁽⁵⁾ | See ⁽⁶⁾ | | | 1 | | pF |
| t _{START, LFXT} | Startup time ⁽⁷⁾ | f _{OSC} = 32768 Hz LFXTBYPASS = 0, LFXTDRIVE = {3}, T _A = 25°C, C _{L,eff} = 12.5 pF | | | 1000 | | ms |
| f _{Fault, LFXT} | Oscillator fault frequency ⁽⁸⁾ | XTS = 0 ⁽⁹⁾ | | 0 | | 3500 | Hz |

- (1) To improve EMI on the LFXT oscillator, the following guidelines should be observed.
 - Keep the trace between the device and the crystal as short as possible.
 - Design a good ground plane around the oscillator pins.
 - Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
 - Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
 - Use assembly materials and processes that avoid any parasitic load on the oscillator XIN and XOUT pins.
 - If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.
- (2) When LFXTBYPASS is set, LFXT circuits are automatically powered down. Input signal is a digital square wave with parametrics defined in the Schmitt-trigger inputs section of this data sheet. Duty cycle requirements are defined by DC_{LFXT, SW}.
- (3) Maximum frequency of operation of the entire device cannot be exceeded.
- (4) Oscillation allowance is based on a safety factor of 5 for recommended crystals. The oscillation allowance is a function of the LFXTDRIVE settings and the effective load. In general, comparable oscillator allowance can be achieved based on the following guidelines, but should be evaluated based on the actual crystal selected for the application:
 - For LFXTDRIVE = {0}, C_{L,eff} = 3.7 pF.
 - For LFXTDRIVE = {1}, 6 pF ≤ C_{L,eff} ≤ 9 pF.
 - For LFXTDRIVE = {2}, 6 pF ≤ C_{L,eff} ≤ 10 pF.
 - For LFXTDRIVE = {3}, 6 pF ≤ C_{L,eff} ≤ 12 pF.
- (5) Includes parasitic bond and package capacitance (approximately 2 pF per pin).
- (6) Requires external capacitors at both terminals. Values are specified by crystal manufacturers.
- (7) Includes startup counter of 1024 clock cycles.
- (8) Frequencies above the MAX specification do not set the fault flag. Frequencies in between the MIN and MAX specification may set the flag. A static condition or stuck at fault condition sets the flag.
- (9) Measured with logic-level input frequency but also applies to operation with crystals.

Table 5-4. DCO FLL, Frequency

Over recommended operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|------------------------|--|--|-----------------|-------|--------|------|------|
| f _{DCO, FLL} | FLL lock frequency, 16 MHz, 25°C | Measured at MCLK, Internal trimmed REFO as reference | 3 V | -1.0% | | 1.0% | |
| | FLL lock frequency, 16 MHz, -40°C to +85°C | | 3 V | -2.0% | | 2.0% | |
| | FLL lock frequency, 16 MHz, -40°C to +85°C | Measured at MCLK, XT1 crystal as reference | 3 V | -0.5% | | 0.5% | |
| f _{DUTY} | Duty cycle | Measured at MCLK, XT1 crystal as reference | 3 V | 40% | 50% | 60% | |
| Jitter _{CC} | Cycle-to-cycle jitter, 16 MHz | | 3 V | | 0.25% | | |
| Jitter _{long} | Long-term jitter, 16 MHz | | 3 V | | 0.022% | | |
| t _{FLL, lock} | FLL lock time | | 3 V | | 120 | | ms |

Table 5-5. REFO

Over recommended operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|--------------------------------------|-------------------------------------|---|-----------------|-------|-------|-------|------|
| I _{REFO} | REFO oscillator current consumption | T _A = 25°C | 3 V | | 15 | | μA |
| f _{REFO} | REFO calibrated frequency | Measured at MCLK | 3 V | | 32768 | | Hz |
| | REFO absolute calibrated tolerance | -40°C – +85°C | 1.8 V to 3.6 V | -3.5% | | +3.5% | |
| df _{REFO} /dT | REFO frequency temperature drift | Measured at MCLK ⁽¹⁾ | 3 V | | 0.01 | | %/°C |
| df _{REFO} /dV _{CC} | REFO frequency supply voltage drift | Measured at MCLK at 25°C ⁽²⁾ | 1.8 V to 3.6 V | | 1 | | %/V |
| f _{DC} | REFO duty cycle | Measured at MCLK | 1.8 V to 3.6 V | 40% | 50% | 60% | |
| t _{START} | REFO startup time | 40% to 60% duty cycle | | | 50 | | μs |

(1) Calculated using the box method: (MAX(-40 to 85°C) – MIN(-40 to 85°C)) / MIN(-40 to 85°C) / (85°C – (-40°C))

(2) Calculated using the box method: (MAX(1.8 to 3.6 V) – MIN(1.8 to 3.6 V)) / MIN(1.8 to 3.6 V) / (3.6 V – 1.8 V)

Table 5-6. Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-------------------------------------|------------------------------------|---------------------------------|-----------------|-----|-----|-----|------|
| f _{VLO} | VLO frequency | Measured at MCLK | 3 V | | 10 | | kHz |
| df _{VLO} /dT | VLO frequency temperature drift | Measured at MCLK ⁽¹⁾ | 3 V | | 0.5 | | %/°C |
| df _{VLO} /dV _{CC} | VLO frequency supply voltage drift | Measured at MCLK ⁽²⁾ | 1.8 V to 3.6 V | | 4 | | %/V |
| f _{VLO,DC} | Duty cycle | Measured at MCLK | 3 V | | 50% | | |

(1) Calculated using the box method: (MAX(-40 to 85°C) – MIN(-40 to 85°C)) / MIN(-40 to 85°C) / (85°C – (-40°C))

(2) Calculated using the box method: (MAX(1.8 to 3.6 V) – MIN(1.8 to 3.6 V)) / MIN(1.8 to 3.6 V) / (3.6 V – 1.8 V)

Table 5-7. Module Oscillator (MODOSC)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|---------------------------------------|---------------------------------------|-----------------|-----------------|-----|-------|-----|------|
| f _{MODOSC} | MODOSC frequency | | 3 V | 3.8 | 4.8 | 5.8 | MHz |
| f _{MODOSC} /dT | MODOSC frequency temperature drift | | 3 V | | 0.102 | | %/°C |
| f _{MODOSC} /dV _{CC} | MODOSC frequency supply voltage drift | | 1.8 V to 3.6 V | | 1.02 | | %/V |
| f _{MODOSC,DC} | Duty cycle | | 3 V | 40% | 50% | 60% | |

5.12.4 Digital I/Os

Table 5-8. Digital Inputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|------------------------|---|-----------------|------|-----|------|------|
| V _{IT+} | Positive-going input threshold voltage | 2 V | 0.90 | | 1.50 | V |
| | | 3 V | 1.35 | | 2.25 | |
| V _{IT-} | Negative-going input threshold voltage | 2 V | 0.50 | | 1.10 | V |
| | | 3 V | 0.75 | | 1.65 | |
| V _{hys} | Input voltage hysteresis (V _{IT+} – V _{IT-}) | 2 V | 0.3 | | 0.8 | V |
| | | 3 V | 0.4 | | 1.2 | |
| R _{Pull} | Pullup or pulldown resistor For pullup: V _{IN} = V _{SS} For pulldown: V _{IN} = V _{CC} | | 20 | 35 | 50 | kΩ |
| C _{I,dig} | Input capacitance, digital only port pins V _{IN} = V _{SS} or V _{CC} | | | 3 | | pF |
| C _{I,ana} | Input capacitance, port pins with shared analog functions V _{IN} = V _{SS} or V _{CC} | | | 5 | | pF |
| I _{lkg(Px.y)} | High-impedance leakage current (also refer to ⁽¹⁾ and ⁽²⁾) | 2 V, 3 V | -20 | | +20 | nA |

(1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pins, unless otherwise noted.

(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup or pulldown resistor is disabled.

Table 5-9. Digital Outputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------------|--|-----------------|-----|-----|------|------|
| V _{OH} | High-level output voltage I _(OHmax) = -3 mA ⁽¹⁾ | 2 V | 1.4 | | 2.0 | V |
| | | 3 V | 2.4 | | 3.0 | |
| V _{OL} | Low-level output voltage I _(OLmax) = 3 mA ⁽¹⁾ | 2 V | 0.0 | | 0.60 | V |
| | | 3 V | 0.0 | | 0.60 | |
| f _{Port_CLK} | Clock output frequency C _L = 20 pF ⁽²⁾ | 2 V | 16 | | | MHz |
| | | 3 V | 16 | | | |
| t _{rise,dig} | Port output rise time, digital only port pins C _L = 20 pF | 2 V | | 10 | | ns |
| | | 3 V | | 7 | | |
| t _{fall,dig} | Port output fall time, digital only port pins C _L = 20 pF | 2 V | | 10 | | ns |
| | | 3 V | | 5 | | |

(1) The maximum total current, I_(OHmax) and I_(OLmax), for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.

(2) The port can output frequencies at least up to the specified limit and might support higher frequencies.

5.12.4.1 Digital I/O Typical Characteristics

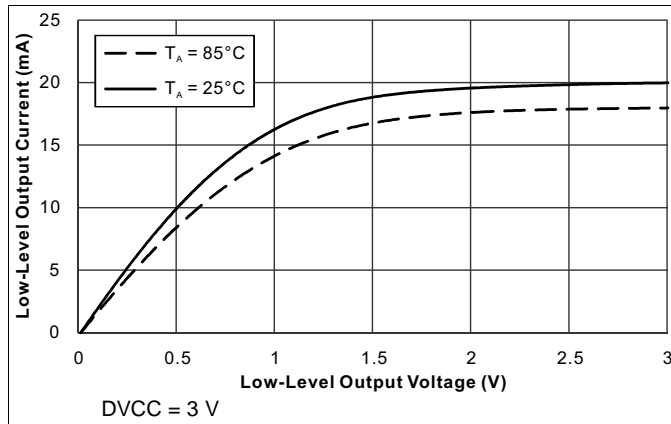


Figure 5-6. Typical Low-Level Output Current vs Low-Level Output Voltage

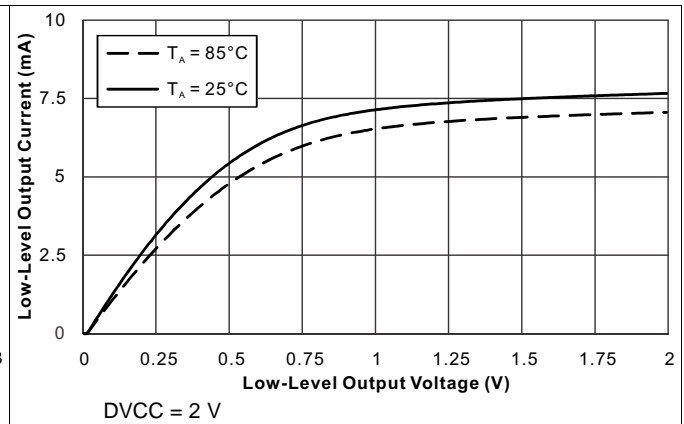


Figure 5-7. Typical Low-Level Output Current vs Low-Level Output Voltage

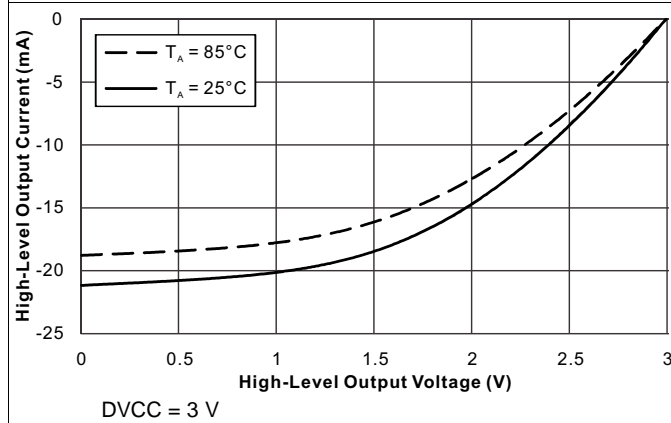


Figure 5-8. Typical High-Level Output Current vs High-Level Output Voltage

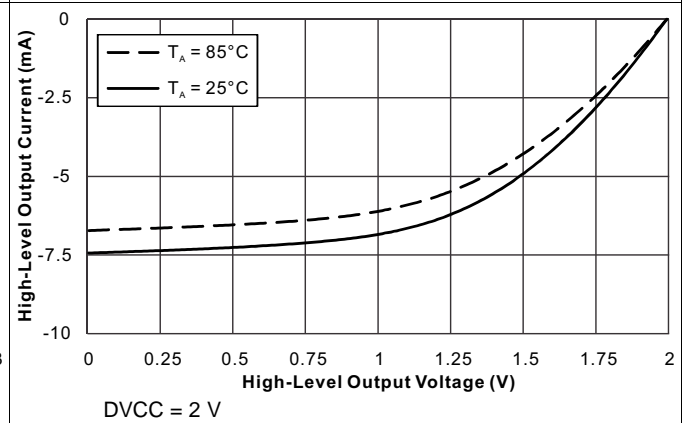


Figure 5-9. Typical High-Level Output Current vs High-Level Output Voltage

PRODUCT PREVIEW

5.12.5 Timer_A

Table 5-10. Timer_A Recommended Operating Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | MAX | UNIT |
|-----------------|-------------------------------|--|-----------------|-----|-----|------|
| f _{TA} | Timer_A input clock frequency | Internal: SMCLK, ACLK External: TACLK Duty cycle = 50% ± 10% | 2 V, 3 V | | 16 | MHz |

5.12.6 eUSCI

Table 5-11. eUSCI (UART Mode) Recommended Operating Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | MAX | UNIT |
|---------------------|---|---|-----------------|-----|-----|------|
| f _{eUSCI} | eUSCI input clock frequency | Internal: SMCLK, MODCLK External: UCLK Duty cycle = 50% ± 10% | 2 V, 3 V | | 16 | MHz |
| f _{BITCLK} | BITCLK clock frequency (equals baud rate in Mbaud) | | 2 V, 3 V | | 5 | MHz |

Table 5-12. eUSCI (UART Mode) Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | TYP | UNIT |
|----------------|---|-------------------------|-----------------|-----|------|
| t _t | UART receive deglitch time ⁽¹⁾ | UCGLIT _x = 0 | 2 V, 3 V | 12 | ns |
| | | UCGLIT _x = 1 | | 40 | |
| | | UCGLIT _x = 2 | | 68 | |
| | | UCGLIT _x = 3 | | 110 | |

- (1) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized their width should exceed the maximum specification of the deglitch time.

Table 5-13. eUSCI (SPI Master Mode) Recommended Operating Conditions

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | CONDITIONS | MIN | MAX | UNIT |
|--------------------|-----------------------------|---|-----|-----|------|
| f _{eUSCI} | eUSCI input clock frequency | Internal: SMCLK, MODCLK Duty cycle = 50% ± 10% | | 8 | MHz |

Table 5-14. eUSCI (SPI Master Mode) Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see Note ⁽¹⁾)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | MAX | UNIT |
|-----------------------|--|--|-----------------|-----|-----|---------------|
| t _{STE,LEAD} | STE lead time, STE active to clock | UCSTEM = 1, UCMODE _x = 01 or 10 | | 1 | | UCxCLK cycles |
| t _{STE,LAG} | STE lag time, Last clock to STE inactive | UCSTEM = 1, UCMODE _x = 01 or 10 | | 1 | | UCxCLK cycles |
| t _{SU,MI} | SOMI input data setup time | | 2 V | 45 | | ns |
| | | | 3 V | 35 | | |
| t _{HD,MI} | SOMI input data hold time | | 2 V | 0 | | ns |
| | | | 3 V | 0 | | |
| t _{VALID,MO} | SIMO output data valid time ⁽²⁾ | UCLK edge to SIMO valid, C _L = 20 pF | 2 V | | 20 | ns |
| | | | 3 V | | 20 | |
| t _{HD,MO} | SIMO output data hold time ⁽³⁾ | C _L = 20 pF | 2 V | 0 | | ns |
| | | | 3 V | 0 | | |

- (1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} = \max(t_{VALID,MO(eUSCI)} + t_{SU,SI(Slave)}, t_{SU,MI(eUSCI)} + t_{VALID,SO(Slave)})$.
For the slave's parameters $t_{SU,SI(Slave)}$ and $t_{VALID,SO(Slave)}$ refer to the SPI parameters of the attached slave.
- (2) Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. Refer to the timing diagrams in [Figure 5-10](#) and [Figure 5-11](#).
- (3) Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. Refer to the timing diagrams in [Figure 5-10](#) and [Figure 5-11](#).

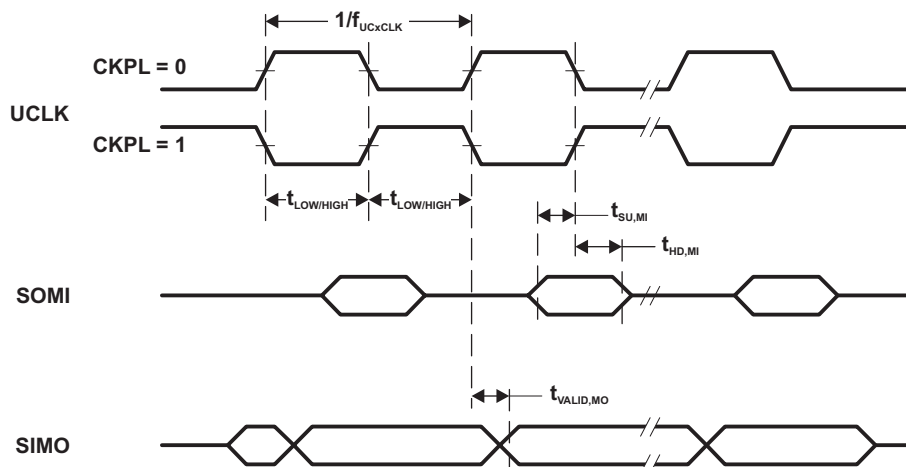


Figure 5-10. SPI Master Mode, CKPH = 0

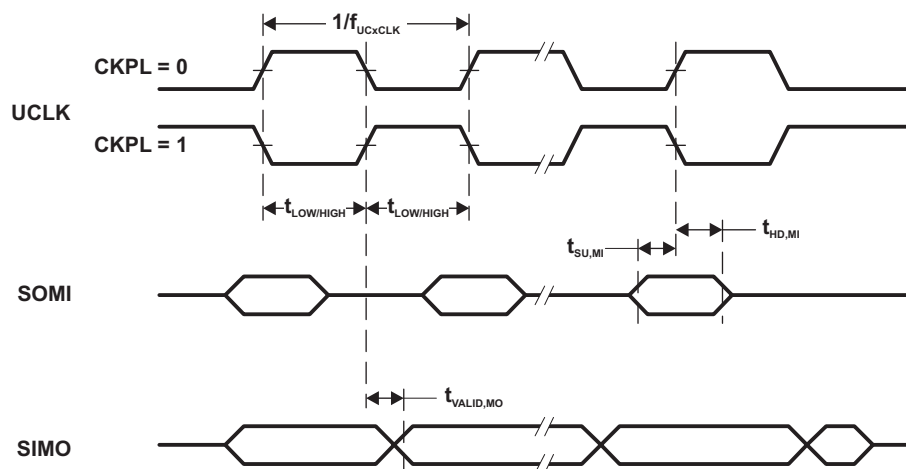


Figure 5-11. SPI Master Mode, CKPH = 1

Table 5-15. eUSCI (SPI Slave Mode) Switching Characteristicsover recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | MAX | UNIT |
|-----------------------|---|--|-----------------|-----|-----|------|
| t _{STE,LEAD} | STE lead time, STE active to clock | | 2 V | 40 | | ns |
| | | | 3 V | 24 | | |
| t _{STE,LAG} | STE lag time, Last clock to STE inactive | | 2 V | 20 | | ns |
| | | | 3 V | 20 | | |
| t _{STE,ACC} | STE access time, STE active to SOMI data out | | 2 V | | 65 | ns |
| | | | 3 V | | 40 | |
| t _{STE,DIS} | STE disable time, STE inactive to SOMI high impedance | | 2 V | | 40 | ns |
| | | | 3 V | | 35 | |
| t _{SU,SI} | SIMO input data setup time | | 2 V | 4 | | ns |
| | | | 3 V | 4 | | |
| t _{HD,SI} | SIMO input data hold time | | 2 V | 12 | | ns |
| | | | 3 V | 12 | | |
| t _{VALID,SO} | SOMI output data valid time ⁽²⁾ | UCLK edge to SOMI valid, C _L = 20 pF | 2 V | | 55 | ns |
| | | | 3 V | | 30 | |
| t _{HD,SO} | SOMI output data hold time ⁽³⁾ | C _L = 20 pF | 2 V | 5 | | ns |
| | | | 3 V | 5 | | |

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(eUSCI)}, t_{SU,MI(Master)} + t_{VALID,SO(eUSCI)})$.For the master's parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$ refer to the SPI parameters of the attached slave.(2) Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. Refer to the timing diagrams in [Figure 5-12](#) and [Figure 5-13](#).(3) Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. Refer to the timing diagrams in [Figure 5-12](#) and [Figure 5-13](#).

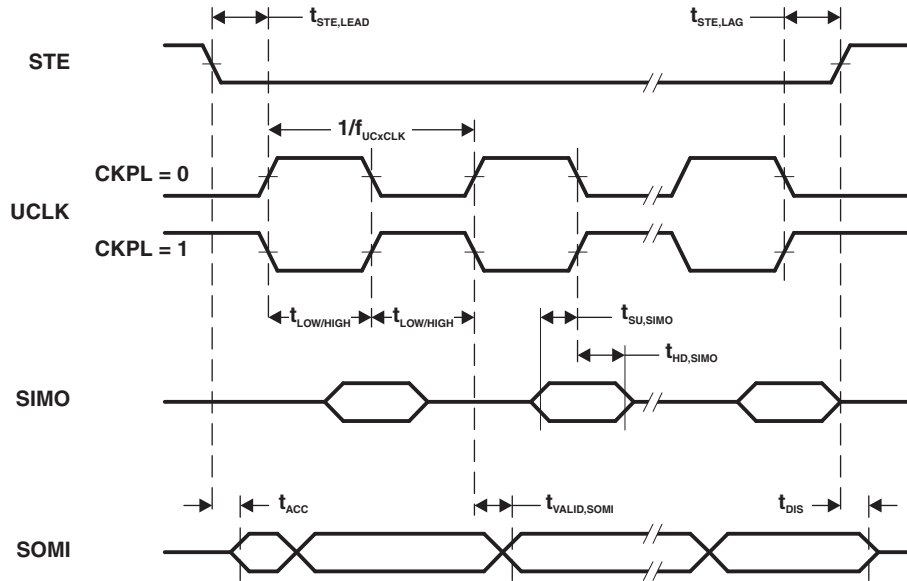


Figure 5-12. SPI Slave Mode, CKPH = 0

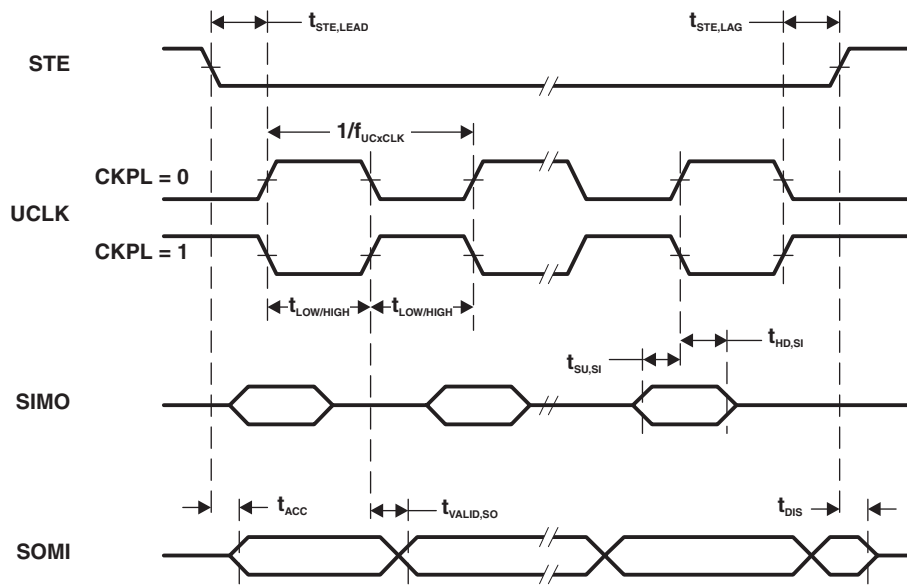


Figure 5-13. SPI Slave Mode, CKPH = 1

Table 5-16. eUSCI (I²C Mode) Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 5-14](#))

| PARAMETER | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT | |
|----------------------|---|----------------------------|-------------|------|-----|------|----|
| f _{eUSCI} | eUSCI input clock frequency | | | | 16 | MHz | |
| f _{SCL} | SCL clock frequency | 2 V, 3 V | 0 | | 400 | kHz | |
| t _{HD,STA} | Hold time (repeated) START | f _{SCL} = 100 kHz | 4.0 | | | μs | |
| | | f _{SCL} > 100 kHz | 0.6 | | | | |
| t _{SU,STA} | Setup time for a repeated START | f _{SCL} = 100 kHz | 4.7 | | | μs | |
| | | f _{SCL} > 100 kHz | 0.6 | | | | |
| t _{HD,DAT} | Data hold time | 2 V, 3 V | 0 | | | ns | |
| t _{SU,DAT} | Data setup time | 2 V, 3 V | 250 | | | ns | |
| t _{SU,STO} | Setup time for STOP | f _{SCL} = 100 kHz | 4.0 | | | μs | |
| | | f _{SCL} > 100 kHz | 0.6 | | | | |
| t _{SP} | Pulse duration of spikes suppressed by input filter | 2 V, 3 V | UCGLITx = 0 | 50 | | 600 | ns |
| | | | UCGLITx = 1 | 25 | | 300 | ns |
| | | | UCGLITx = 2 | 12.5 | | 150 | ns |
| | | | UCGLITx = 3 | 6.3 | | 75 | ns |
| t _{TIMEOUT} | Clock low timeout | 2 V, 3 V | UCCLTOx = 1 | 27 | | | ms |
| | | | UCCLTOx = 2 | 30 | | | ms |
| | | | UCCLTOx = 3 | 33 | | | ms |

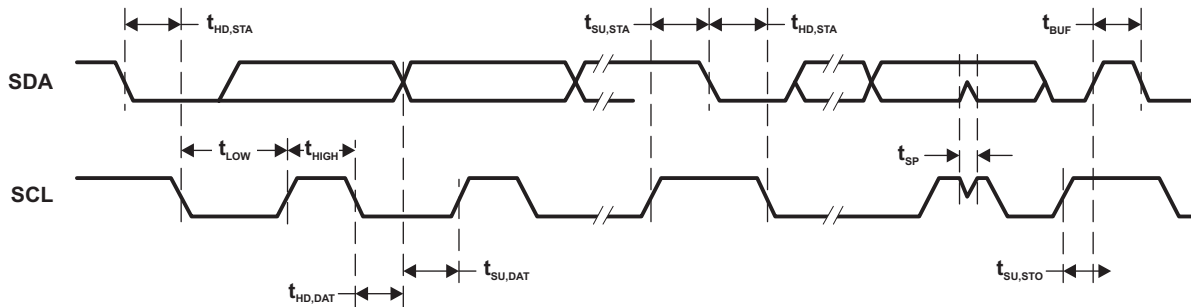


Figure 5-14. I²C Mode Timing

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5.12.7 ADC

Table 5-17. ADC, Power Supply and Input Range Conditions

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|-------------------|---|--|-----------------|-----|-----|------------------|------|
| DV _{CC} | ADC supply voltage | | | 2.0 | | 3.6 | V |
| V _(Ax) | Analog input voltage range | All ADC pins | | 0 | | DV _{CC} | V |
| I _{ADC} | Operating supply current into DV _{CC} terminal, reference current not included, repeat-single-channel mode | f _{ADCCLK} = 5 MHz, ADCON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADCDIV = 0, ADCCONSEQx = 10b | 2 V | 185 | | | μA |
| | | | 3 V | 207 | | | |
| C ₁ | Input capacitance | Only one terminal Ax can be selected at one time from the pad to the ADC capacitor array, including wiring and pad | 2.2 V | | 1.6 | 2.0 | pF |
| R ₁ | Input MUX ON resistance | DV _{CC} = 2 V, 0 V = V _{Ax} = DV _{CC} | | | | 2 | kΩ |

Table 5-18. ADC, 10-Bit Timing Parameters

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|----------------------|----------------------------------|---|-----------------|------|-----|------|------|
| f _{ADCCLK} | | For specified performance of ADC linearity parameters | 2 V to 3.6 V | 0.45 | 5 | 5.5 | MHz |
| f _{ADCOSC} | Internal ADC oscillator (MODOSC) | ADCDIV = 0, f _{ADCCLK} = f _{ADCOSC} | 2 V to 3.6 V | 4.5 | 4.5 | 5.5 | MHz |
| t _{CONVERT} | Conversion time | REFON = 0, Internal oscillator, 10 ADCCLK cycles, 10-bit mode, f _{ADCOSC} = 4.5 MHz to 5.5 MHz | 2 V to 3.6 V | 2.18 | | 2.67 | μs |
| | | External f _{ADCCLK} from ACLK, MCLK, or SMCLK, ADCSSEL ≠ 0 | 2 V to 3.6 V | (1) | | | |
| t _{ADCON} | Turn on settling time of the ADC | The error in a conversion started after t _{ADCON} is less than ±0.5 LSB, Reference and input signal already settled | | | | 100 | ns |
| t _{Sample} | Sampling time | R _S = 1000 Ω, R ₁ = 36000 Ω, C ₁ = 3.5 pF, Approximately eight Tau (t) are required for an error of less than ±0.5 LSB | 2 V | 1.5 | | | μs |
| | | | 3 V | 2.0 | | | |

(1) 12 × ADCDIV × 1/f_{ADCCLK}

Table 5-19. ADC, 10-Bit Linearity Parameters

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | V _{CC} | MIN | TYP | MAX | UNIT |
|---------------------------------|---|--|-----------------|-------|-------|------|-------|
| E _I | Integral linearity error (10-bit mode) | V _{DVCC} as reference | 2.4 V to 3.6 V | -2 | | 2 | LSB |
| | Integral linearity error (8-bit mode) | | 2 V to 3.6 V | -2 | | 2 | |
| E _D | Differential linearity error (10-bit mode) | V _{DVCC} as reference | 2.4 V to 3.6 V | -1 | | 1 | LSB |
| | Differential linearity error (8-bit mode) | | 2 V to 3.6 V | -1 | | 1 | |
| E _O | Offset error (10-bit mode) | V _{DVCC} as reference | 2.4 V to 3.6 V | -6.5 | | 6.5 | mV |
| | Offset error (8-bit mode) | | 2 V to 3.6 V | -6.5 | | 6.5 | |
| E _G | Gain error (10-bit mode) | V _{DVCC} as reference | 2.4 V to 3.6 V | -2.0 | | 2.0 | LSB |
| | | Internal 1.5-V reference | | -3.0% | | 3.0% | |
| | Gain error (8-bit mode) | V _{DVCC} as reference | 2 V to 3.6 V | -2.0 | | 2.0 | LSB |
| | | Internal 1.5-V reference | | -3.0% | | 3.0% | |
| E _T | Total unadjusted error (10-bit mode) | V _{DVCC} as reference | 2.4 V to 3.6 V | -2.0 | | 2.0 | LSB |
| | | Internal 1.5-V reference | | -3.0% | | 3.0% | |
| | Total unadjusted error (8-bit mode) | V _{DVCC} as reference | 2 V to 3.6 V | -2.0 | | 2.0 | LSB |
| | | Internal 1.5-V reference | | -3.0% | | 3.0% | |
| V _{SENSOR} | See ⁽¹⁾ | ADCON = 1, INCH = 0Ch, T _A = 0°C | 3 V | | 1.013 | | mV |
| TC _{SENSOR} | See ⁽²⁾ | ADCON = 1, INCH = 0Ch | 3 V | | 3.35 | | mV/°C |
| t _{SENSOR} (sample) | Sample time required if channel 12 is selected ⁽³⁾ | ADCON = 1, INCH = 0Ch, Error of conversion result ≤ 1 LSB, AM and all LPM above LPM3 | 3 V | | 30 | | μs |
| | | ADCON = 1, INCH = 0Ch, Error of conversion result ≤ 1 LSB, LPM3 | 3 V | | 100 | | |

- (1) The temperature sensor offset can vary significantly. A single-point calibration is recommended to minimize the offset error of the built-in temperature sensor.
- (2) The device descriptor structure contains calibration values for 30°C ± 3°C and 85°C ± 3°C for each of the available reference voltage levels. The sensor voltage can be computed as V_{SENSE} = TC_{SENSOR} × (Temperature, °C) + V_{SENSOR}, where TC_{SENSOR} and V_{SENSOR} can be computed from the calibration values for higher accuracy.
- (3) The typical equivalent impedance of the sensor is 700 kΩ. The sample time required includes the sensor-on time t_{SENSOR(on)}.

5.12.8 LCD Controller

Table 5-20. LCD Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| PARAMETER | CONDITIONS | MIN | NOM | MAX | UNIT | |
|-------------------------|--|--|-----|------|---------------|-----|
| $V_{CC,LCD,CP\ en,3.6}$ | Supply voltage range, charge pump enabled, $V_{LCD} \leq 3.6\text{ V}$ | 1.8 | | 3.6 | V | |
| $V_{CC,LCD,ext.\ bias}$ | Supply voltage range, external biasing, charge pump enabled | 1.8 | | 3.6 | V | |
| $V_{CC,LCD,VLCD\ EXT}$ | Supply voltage range, external LCD voltage, external biasing, charge pump disabled | 1.8 | | 3.6 | V | |
| V_{R33} | External LCD voltage at LCDCAP/R33, external biasing, charge pump disabled | 2.4 | | 3.6 | V | |
| C_{LCDCAP} | | | 0.1 | | μF | |
| C_{R33} | | | 0.1 | | μF | |
| C_{R23} | | | 0.1 | | μF | |
| C_{R13} | | | 0.1 | | μF | |
| f_{Frame} | LCD frame frequency range | $f_{LCD} = 2 \times \text{MUX} \times f_{FRAME}$ with $\text{MUX} = 1$ (static), 2, 3, 4 | 16 | 32 | 64 | Hz |
| $f_{ACLK,in}$ | ACLK input frequency range | | 30 | 32 | 40 | kHz |
| C_{Panel} | Panel capacitance | | | 8000 | pF | |
| V_{R33} | Analog input voltage at R33 | LCDCPEN = 0, LCDSELVDD = 0, LCDREFEN = 0 | 2.4 | | 3.6 | V |
| $V_{R23,1/3bias}$ | Analog input voltage at R23 | LCDCPEN = 0, LCDSELVDD = 0, LCDREFEN = 0 | 1.2 | | 2.4 | V |
| $V_{R13,1/3bias}$ | Analog input voltage at R13 with 1/3 biasing | | 0.0 | | 1.2 | V |
| $V_{LCDREF/R13}$ | External LCD reference voltage applied at LCDREF/R13 | LCDCPEN=1, LCDSELVDD=0, LCDREFEN = 0 | 0.8 | 1.0 | 1.2 | V |

5.12.9 FRAM

Table 5-21. FRAM

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | MAX | UNIT |
|--------------------------|-------------------------|-----------------------|------------------|-----|--------|
| Read and write endurance | | | 10 ¹⁵ | | cycles |
| t _{Retention} | Data retention duration | T _J = 25°C | 100 | | years |
| | | T _J = 70°C | 40 | | |
| | | T _J = 85°C | 10 | | |

5.12.10 Emulation and Debug

Table 5-22. JTAG and Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

| PARAMETER | | V _{CC} | MIN | TYP | MAX | UNIT |
|-----------------------|--|-----------------|-------|-----|-----|------|
| f _{SBW} | Spy-Bi-Wire input frequency | 2 V, 3 V | 0 | | 10 | MHz |
| t _{SBW,Low} | Spy-Bi-Wire low clock pulse duration | 2 V, 3 V | 0.028 | | 15 | μs |
| t _{SBW,En} | Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge) ⁽¹⁾ | 2 V, 3 V | | | 110 | μs |
| t _{SBW,Rst} | Spy-Bi-Wire return to normal operation time | | 15 | | 100 | μs |
| f _{TCK} | TCK input frequency - 4-wire JTAG ⁽²⁾ | 2 V | 0 | | 16 | MHz |
| | | 3 V | 0 | | 16 | MHz |
| R _{Internal} | Internal pulldown resistance on TEST | 2 V, 3 V | 20 | 35 | 50 | kΩ |

- (1) Tools that access the Spy-Bi-Wire interface must wait for the t_{SBW,En} time after pulling the TEST/SBWTCK pin high before applying the first SBWTCK clock edge.
- (2) f_{TCK} may be restricted to meet the timing requirements of the module selected.

6 Detailed Description

6.1 CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter (PC), stack pointer (SP), status register (SR), and constant generator (CG), respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

6.2 Operating Modes

The MSP430 has one active mode and several software selectable low-power modes of operation. An interrupt event can wake up the device from low-power mode LPM0 or LPM3, service the request, and restore back to the low-power mode on return from the interrupt program. Low-power modes LPM3.5 and LPM4.5 disable the core supply to minimize power consumption.

Table 6-1. Operating Modes

| MODE | | AM | LPM0 | LPM3 | LPM4 | LPM3.5 | LPM4.5 |
|--------------------------------|------------------------------|-----------------|-----------------|--------------------|-------------------------|--------------------------|-------------------|
| | | Active Mode | CPU Off | Standby | Off | Only RTC Counter and LCD | Shutdown |
| Maximum System Clock | | 16 MHz | 16 MHz | 40 kHz | 0 | 40 kHz | 0 |
| Power Consumption at 25°C, 3 V | | 100 μ A/MHz | 20 μ A/MHz | 1.2 μ A | 0.6 μ A without SVS | 0.77 μ A | 13 nA without SVS |
| Wake-up time | | N/A | instant | 10 μ s | 10 μ s | 150 μ s | 150 μ s |
| Wake-up events | | N/A | All | All | I/O | RTC Counter I/O | I/O |
| Power | Regulator | Full Regulation | Full Regulation | Partial Power Down | Partial Power Down | Partial Power Down | Power Down |
| | SVS | On | On | Optional | Optional | Optional | Optional |
| | Brown Out | On | On | On | On | On | On |
| Clock | MCLK | Active | Off | Off | Off | Off | Off |
| | SMCLK | Optional | Optional | Off | Off | Off | Off |
| | FLL | Optional | Optional | Off | Off | Off | Off |
| | DCO | Optional | Optional | Off | Off | Off | Off |
| | MODCLK | Optional | Optional | Off | Off | Off | Off |
| | REFO | Optional | Optional | Optional | Off | Off | Off |
| | ACLK | Optional | Optional | Optional | Off | Off | Off |
| | XT1CLK | Optional | Optional | Optional | Off | Optional | Off |
| Core | VLOCLK | Optional | Optional | Optional | Off | Optional | Off |
| | CPU | On | Off | Off | Off | Off | Off |
| | FRAM | On | On | Off | Off | Off | Off |
| | RAM | On | On | On | On | Off | Off |
| | Backup Memory ⁽¹⁾ | On | On | On | On | On | Off |

(1) Backup memory contains one 32-byte register in the peripheral memory space. Refer to [Table 6-29](#) and [Table 6-48](#) for its memory allocation.

Table 6-1. Operating Modes (continued)

| MODE | | AM | LPM0 | LPM3 | LPM4 | LPM3.5 | LPM4.5 |
|-------------|------------------------------|-------------|----------|------------|------------|--------------------------|------------|
| | | Active Mode | CPU Off | Standby | Off | Only RTC Counter and LCD | Shutdown |
| Peripherals | Timer0_A3 | Optional | Optional | Optional | Off | Off | Off |
| | Timer1_A3 | Optional | Optional | Optional | Off | Off | Off |
| | WDT | Optional | Optional | Optional | Off | Off | Off |
| | eUSCI_A0 | Optional | Optional | Off | Off | Off | Off |
| | eUSCI_B0 | Optional | Optional | Off | Off | Off | Off |
| | CRC | Optional | Optional | Off | Off | Off | Off |
| | ADC | Optional | Optional | Optional | Off | Off | Off |
| | LCD | Optional | Optional | Optional | Off | Optional | Off |
| | RTC Counter | Optional | Optional | Optional | Off | Optional | Off |
| I/O | General Digital Input/Output | On | Optional | State Held | State Held | State Held | State Held |
| | Capacitive Touch I/O | Optional | Optional | Optional | Off | Off | Off |

6.3 Interrupt Vector Addresses

The interrupt vectors and the power-up start address are located in the address range 0FFFFh to 0FF80h. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence

Table 6-2. Interrupt Sources, Flags, and Vectors

| INTERRUPT SOURCE | INTERRUPT FLAG | SYSTEM INTERRUPT | WORD ADDRESS | PRIORITY |
|--|---|------------------|--------------|-------------|
| System Reset Power-up, Brownout, Supply Supervisor External Reset RST Watchdog Timeout, Key Violation FRAM uncorrectable bit error detection Software POR, FLL unlock error | SVSHIFG PMMRSTIFG WDTIFG PMMPORIFG, PMMBORIFG SYSRSTIV FLLUNLOCKIFG | Reset | FFFEh | 63, Highest |
| System NMI Vacant Memory Access JTAG Mailbox FRAM access time error FRAM bit error detection | VMAIFG JMBINIFG, JMBOUTIFG ACCTEIFG CBDIFG, UBDIFG | Non-Maskable | FFFCh | 62 |
| User NMI External NMI Oscillator Fault | NMIIIFG OFIFG | Non-Maskable | FFFAh | 61 |
| Timer0_A3 | TA0CCR0 CCIFG0 | Maskable | FFF8h | 60 |
| Timer0_A3 | TA0CCR1 CCIFG1, TA0CCR2 CCIFG2, TA0IFG (TA0IV) | Maskable | FFF6h | 59 |
| Timer1_A3 | TA1CCR0 CCIFG0 | Maskable | FFF4h | 58 |
| Timer1_A3 | TA1CCR1 CCIFG1, TA1CCR2 CCIFG2, TA1IFG (TA1IV) | Maskable | FFF2h | 57 |
| RTC Counter | RTCIFG | Maskable | FFF0h | 56 |
| Watchdog Timer Interval mode | WDTIFG | Maskable | FFEEh | 55 |
| eUSCI_A0 Receive or Transmit | UCTXCFIFG, UCSTTIFG, UCRXIFG, UCTXIFG (UART mode) UCRXIFG, UCTXIFG (SPI mode) (UCA0IV) | Maskable | FFECCh | 54 |

Table 6-2. Interrupt Sources, Flags, and Vectors (continued)

| | | | | |
|------------------------------|--|----------|-------------|------------|
| eUSCI_B0 Receive or Transmit | UCB0RXIFG, UCB0TXIFG (SPI mode) UCALIFG, UCNACKIFG, UCSTTIFG, UCSTPIFG, UCRXIFG0, UCTXIFG0, UCRXIFG1, UCTXIFG1, UCRXIFG2, UCTXIFG2, UCRXIFG3, UCTXIFG3, UCCNTIFG, UCBIT9IFG (I2C mode) (UCB0IV) | Maskable | FFEAh | 53 |
| ADC | ADCIFG0, ADCINIFG, ADCLOIFG, ADCHIIFG, ADCTOVIFG, ADCOVIFG (ADCIV) | Maskable | FFE8h | 52 |
| P1 | P1IFG.0 to P1IFG.7 (P1IV) | Maskable | FFE6h | 51 |
| P2 | P2IFG.0 to P2IFG.7 (P2IV) | Maskable | FFE4h | 50 |
| LCD | LCDBLKOFFIFG, LCDBLKONIFG, LCDFRMIFG (LCDEIV) | Maskable | FFE2h | 49, Lowest |
| Reserved | Reserved | Maskable | FFE0h-FF88h | |
| Signatures | BSL Signature 2 | | 0FF86h | |
| | BSL Signature 1 | | 0FF84h | |
| | JTAG Signature 2 | | 0FF82h | |
| | JTAG Signature 1 | | 0FF80h | |

6.4 Bootstrap Loader (BSL)

The BSL enables users to program the FRAM or RAM using a UART serial interface. Access to the device memory through the BSL is protected by an user-defined password. Use of the BSL requires four pins as shown in [Table 6-3](#). BSL entry requires a specific entry sequence on the $\overline{\text{RST}}/\text{NMISBWDIO}$ and TEST/SBWTCK pins. For a complete description of the features of the BSL and its implementation, see *MSP430 Programming Via the Bootstrap Loader (BSL)* ([SLAU319](#)).

Table 6-3. BSL Pin Requirements and Functions

| DEVICE SIGNAL | BSL FUNCTION |
|--|-----------------------|
| $\overline{\text{RST}}/\text{NMI}/\text{SBWDIO}$ | Entry sequence signal |
| TEST/SBWTCK | Entry sequence signal |
| P1.0 | Data transmit |
| P1.1 | Data receive |
| VCC | Power Supply |
| VSS | Ground Supply |

6.5 JTAG Standard Interface

The MSP430 family supports the standard JTAG interface which requires four signals for sending and receiving data. The JTAG signals are shared with general-purpose I/O. The TEST/SBWTCK pin is used to enable the JTAG signals. In addition to these signals, the $\overline{\text{RST}}/\text{NMI}/\text{SBWDIO}$ is required to interface with MSP430 development tools and device programmers. The JTAG pin requirements are shown in [Table 6-4](#). For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide* ([SLAU278](#)). For a complete description of the features of the JTAG interface and its implementation, see *MSP430 Programming Via the JTAG Interface* ([SLAU320](#)).

Table 6-4. JTAG Pin Requirements and Function

| DEVICE SIGNAL | DIRECTION | JTAG FUNCTION |
|------------------------|-----------|----------------------------|
| P1.4/MCLK/TCK/A4/VREF+ | IN | JTAG clock input |
| P1.5/TA0CLK/TMS/A5 | IN | JTAG state control |
| P1.6/TA0.2/TDI/TCLK/A6 | IN | JTAG data input/TCLK input |
| P1.7/TA0.1/TDO/A7 | OUT | JTAG data output |
| TEST/SBWTCK | IN | Enable JTAG pins |
| RST/NMI/SBWDIO | IN | External Reset |
| VCC | | Power Supply |
| VSS | | Ground Supply |

6.6 Spy-Bi-Wire Interface (SBW)

The MSP430 family supports the two wire Spy-Bi-Wire interface. Spy-Bi-Wire can be used to interface with MSP430 development tools and device programmers. [Table 6-5](#) shows the Spy-Bi-Wire interface pin requirements. For further details on interfacing to development tools and device programmers, refer to the *MSP430 Hardware Tools User's Guide* ([SLAU278](#)).

Table 6-5. Spy-Bi-Wire Pin Requirements and Functions

| DEVICE SIGNAL | DIRECTION | SBW FUNCTION |
|----------------|-----------|-------------------------------|
| TEST/SBWTCK | IN | Spy-Bi-Wire clock input |
| RST/NMI/SBWDIO | IN, OUT | Spy-Bi-Wire data input/output |
| VCC | | Power Supply |
| VSS | | Ground Supply |

6.7 FRAM

The FRAM can be programmed using the JTAG port, Spy-Bi-Wire (SBW), the BSL, or in-system by the CPU. Features of the FRAM include:

- Byte and word access capability
- Programmable wait state generation
- Error correction coding (ECC)

6.8 Memory Protection

The device features memory protection that can restrict user access and enable write protection:

- Securing the whole memory map to prevent unauthorized access from JTAG port or BSL, by writing JTAG and BSL signatures using the JTAG port, SBW, the BSL, or in-system by the CPU.
- Write protection enabled to prevent unwanted write operation to FRAM contents by setting the control bits in System Configuration register 0. For more detailed information, refer to the SYS chapter in the *MSP430FR4xx and MSP430FR2xx Family User's Guide* ([SLAU445](#)).

NOTE

The FRAM is protected by default on PUC. To write to FRAM during code execution, the application must first clear the corresponding PFWP or DFWP bit in System Configuration Register 0 to unprotect the FRAM.

6.9 Peripherals

Peripherals are connected to the CPU through data, address, and control buses. All peripherals can be handled by using all instructions in the memory map. For complete module description, see the *MSP430FR4xx and MSP430FR2xx Family User's Guide* ([SLAU445](#)).

6.9.1 Power Management Module (PMM) and On-chip Reference Voltages

The PMM includes an integrated voltage regulator that supplies the core voltage to the device. The PMM also includes supply voltage supervisor (SVS) and brownout protection. The brownout reset circuit (BOR) is implemented to provide the proper internal reset signal to the device during power-on and power-off. The SVS circuitry detects if the supply voltage drops below a user-selectable safe level. SVS circuitry is available on the primary supply.

The device contains two on-chip reference: 1.5 V for internal reference and 1.2 V for external reference.

The 1.5-V reference is internally connected to ADC channel 13. DVCC is internally connected to ADC channel 15. When DVCC is set as the reference voltage for ADC conversion, the DVCC can be easily represent as Equation 1 by using ADC sampling 1.5-V reference without any external components support.

$$DVCC = (1023 \times 1.5 \text{ V}) \div 1.5 \text{ V Reference ADC result} \quad (1)$$

A 1.2-V reference voltage can be buffered and output to P1.4/MCLK/TCK/A4/VREF+, when the ADC channel 4 is selected as the function. For more detailed information, refer to the *MSP430FR4xx and MSP430FR2xx Family User's Guide (SLAU445)*.

6.9.2 Clock System (CS) and Clock Distribution

The clock system includes a 32-kHz crystal oscillator (XT1), an internal very low-power low-frequency oscillator (VLO), an integrated 32-kHz RC oscillator (REFO), an integrated internal digitally controlled oscillator (DCO) that may use frequency-locked loop (FLL) locking with internal or external 32-kHz reference clock, and on-chip asynchronous high-speed clock (MODOSC). The clock system is designed to target cost-effective designs with minimal external components. A fail-safe mechanism is designed for XT1. The clock system module offers the following clock signals.

- Main Clock (MCLK): the system clock used by the CPU and all relevant peripherals accessed by the bus. All clock sources except MODOSC can be selected as the source with a pre-divider of 1, 2, 4, 8, 16, 32, 64, or 128.
- Sub-Main Clock (SMCLK): the subsystem clock used by the peripheral modules. SMCLK derives from the MCLK with a pre-divider of 1, 2, 4, or 8. This means SMCLK is always equal to or less than MCLK.
- Auxiliary Clock (ACLK): this clock is derived from the external XT1 clock or internal REFO clock up to 40 kHz.

All peripherals may have one or several clock sources depending on specific functionality. Table 6-6 shows the clock distribution used in this device.

Table 6-6. Clock Distribution

| | Clock Source Select Bits | MCLK | SMCLK | ACLK | MODCLK | XT1CLK | VLOCLK | EXTERNAL PIN |
|-----------------|--------------------------|--------------|--------------|--------------|-------------|--------------|--------------|-------------------|
| Frequency Range | | DC to 16 MHz | DC to 16 MHz | DC to 40 kHz | 5 MHz ± 10% | DC to 40 kHz | 10 kHz ± 50% | |
| CPU | N/A | Default | | | | | | |
| FRAM | N/A | Default | | | | | | |
| RAM | N/A | Default | | | | | | |
| CRC | N/A | Default | | | | | | |
| I/O | N/A | Default | | | | | | |
| TA0 | TASSEL | | 10b | 01b | | | | 00b (TA0CLK pin) |
| TA1 | TASSEL | | 10b | 01b | | | | 00b (TA1CLK pin) |
| eUSCI_A0 | UCSSEL | | 10b or 11b | | 01b | | | 00b (UCA0CLK pin) |
| eUSCI_B0 | UCSSEL | | 10b or 11b | | 01b | | | 00b (UCB0CLK pin) |
| WDT | WDTSEL | | 00b | 01b | | | 10b | |
| ADC | ADCSEL | | 11b | 01b | 00b | | | |

Table 6-6. Clock Distribution (continued)

| | Clock Source Select Bits | MCLK | SMCLK | ACLK | MODCLK | XT1CLK | VLOCLK | EXTERNAL PIN |
|-----|--------------------------|------|-------|------|--------|--------|--------|--------------|
| LCD | LCDSSSEL | | | 01b | | 00b | 10b | |
| RTC | RTCSS | | 01b | | | 10b | 11b | |

6.9.3 General-Purpose Input/Output Port (I/O)

There are up to 60 I/O ports implemented.

- P1, P2, P3, P4, P5, P6, and P7 are full 8-bit ports; P8 has 4 bits implemented.
- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Programmable pullup or pulldown on all ports.
- Edge-selectable interrupt and LPM3.5 and LPM4.5 wake-up input capability is available for P1 and P2.
- Read and write access to port-control registers is supported by all instructions.
- Ports can be accessed byte-wise or word-wise in pairs.
- Capacitive Touch IO functionality is supported on all pins.

NOTE

Configuration of digital I/Os after BOR reset

To prevent any cross currents during start-up of the device, all port pins are high-impedance with Schmitt triggers and module functions disabled. To enable the I/O functions after a BOR reset, the ports must be configured first and then the LOCKLPM5 bit must be cleared. For details, refer to the *Configuration After Reset* section in the Digital I/O chapter of the *MSP430FR4xx and MSP430FR2xx Family User's Guide* ([SLAU445](#))

6.9.4 Watchdog Timer (WDT)

The primary function of the WDT module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as interval timer and can generate interrupts at selected time intervals.

Table 6-7. WDT Clocks

| WDTSELx | NORMAL OPERATION (WATCHDOG AND INTERVAL TIMER MODE) |
|---------|---|
| 00 | SMCLK |
| 01 | ACLK |
| 10 | VLOCLK |
| 11 | VLOCLK |

6.9.5 System Module (SYS)

The SYS module handles many of the system functions within the device. These include Power-On Reset (POR) and Power-Up Clear (PUC) handling, NMI source selection and management, reset interrupt vector generators, bootstrap loader entry mechanisms, and configuration management (device descriptors). SYS also includes a data exchange mechanism through SBW called a JTAG mailbox mail box that can be used in the application.

Table 6-8. System Module Interrupt Vector Registers

| INTERRUPT VECTOR REGISTER | ADDRESS | INTERRUPT EVENT | VALUE | PRIORITY |
|---------------------------|------------|---|------------|----------|
| SYSRSTIV, System Reset | 015Eh | No interrupt pending | 00h | |
| | | Brownout (BOR) | 02h | Highest |
| | | RSTIFG $\overline{\text{RST}}$ /NMI (BOR) | 04h | |
| | | PMMSWBOR software BOR (BOR) | 06h | |
| | | LPMx.5 wakeup (BOR) | 08h | |
| | | Security violation (BOR) | 0Ah | |
| | | Reserved | 0Ch | |
| | | SVSHIFG SVSH event (BOR) | 0Eh | |
| | | Reserved | 10h | |
| | | Reserved | 12h | |
| | | PMMSWPOR software POR (POR) | 14h | |
| | | WDTIFG watchdog timeout (PUC) | 16h | |
| | | WDTPW password violation (PUC) | 18h | |
| | | FRCTLPW password violation (PUC) | 1Ah | |
| | | Uncorrectable FRAM bit error detection | 1Ch | |
| | | Peripheral area fetch (PUC) | 1Eh | |
| | | PMMPW PMM password violation (PUC) | 20h | |
| | | Reserved | 22h | |
| FLL unlock (PUC) | 24h | | | |
| Reserved | 26h to 3Eh | Lowest | | |
| SYSSNIV, System NMI | 015Ch | No interrupt pending | 00h | |
| | | SVS low-power reset entry | 02h | Highest |
| | | Uncorrectable FRAM bit error detection | 04h | |
| | | ACCTEIFG access time error | 06h | |
| | | Reserved | 08h | |
| | | Reserved | 0Ah | |
| | | Reserved | 0Ch | |
| | | Reserved | 0Eh | |
| | | Reserved | 10h | |
| | | VMAIFG Vacant memory access | 12h | |
| | | JMBINIFG JTAG mailbox input | 14h | |
| | | JMBOUTIFG JTAG mailbox output | 16h | |
| | | Correctable FRAM bit error detection | 18h | |
| | | Reserved | 1Ah to 1Eh | Lowest |
| SYSUNIV, User NMI | 015Ah | No interrupt pending | 00h | |
| | | NMIFG NMI pin or SVS _H event | 02h | Highest |
| | | OFIFG oscillator fault | 04h | |
| | | Reserved | 06h to 1Eh | Lowest |

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6.9.6 Cyclic Redundancy Check (CRC)

The 16-bit cyclic redundancy check (CRC) module produces a signature based on a sequence of data values and can be used for data checking purposes. The CRC generation polynomial is compliant with CRC-16-CCITT standard of $x^{16} + x^{12} + x^5 + 1$.

6.9.7 Enhanced Universal Serial Communication Interface (eUSCI_A0, eUSCI_B0)

The eUSCI modules are used for serial data communications. The eUSCI_A module supports either UART or SPI communications. The eUSCI_B module supports either SPI or I²C communications. Additionally, eUSCI_A supports automatic baudrate detection and IrDA.

Table 6-9. eUSCI Pin Configurations

| eUSCI_A0 | PIN | UART | SPI |
|----------|------|------------------|------|
| | P1.0 | TXD | SIMO |
| | P1.1 | RXD | SOMI |
| | P1.2 | | SCLK |
| | P1.3 | | STE |
| eUSCI_B0 | PIN | I ² C | SPI |
| | P5.0 | | STE |
| | P5.1 | | SCLK |
| | P5.2 | SDA | SIMO |
| | P5.3 | SCL | SOMI |

6.9.8 Timers (Timer0_A3, Timer1_A3)

The Timer0_A3 and Timer1_A3 modules are 16-bit timers and counters with three capture/compare registers each. Each can support multiple captures or compares, PWM outputs, and interval timing. Each has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers. The CCR0 registers on both TA0 and TA1 are not externally connected and can only be used for hardware period timing and interrupt generation. In Up Mode, they can be used to set the overflow value of the counter.

Table 6-10. Timer0_A3 Signal Connections

| PORT PIN | DEVICE INPUT SIGNAL | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL |
|----------|--------------------------------------|-------------------|--------------|----------------------|---|
| P1.5 | TA0CLK | TACLK | Timer | N/A | |
| | ACLK (internal) | ACLK | | | |
| | SMCLK (internal) | SMCLK | | | |
| | from Capacitive Touch IO (internal) | INCLK | | | |
| | | CCI0A | CCR0 | TA0 | |
| | | CCI0B | | | Timer1_A3 CCI0B input |
| | DVSS | GND | | | |
| | DVCC | VCC | | | |
| P1.7 | TA0.1 | CCI1A | CCR1 | TA1 | TA0.1 |
| | from RTC (internal) | CCI1B | | | Timer1_A3 CCI1B input |
| | DVSS | GND | | | |
| | DVCC | VCC | | | |
| P1.6 | TA0.2 | CCI2A | CCR2 | TA2 | TA0.2 |
| | from Capacitive Touch I/O (internal) | CCI2B | | | Timer1_A3 INCLK Timer1_A3 CCI2B input, IR Input |
| | DVSS | GND | | | |
| | DVCC | VCC | | | |

Table 6-11. Timer1_A3 Signal Connections

| PORT PIN | DEVICE INPUT SIGNAL | MODULE INPUT NAME | MODULE BLOCK | MODULE OUTPUT SIGNAL | DEVICE OUTPUT SIGNAL |
|----------|-----------------------------------|-------------------|--------------|----------------------|----------------------|
| P8.2 | TA1CLK | TACLK | Timer | N/A | |
| | ACLK (internal) | ACLK | | | |
| | SMCLK (internal) | SMCLK | | | |
| | Timer0_A3 CCR2B output (internal) | INCLK | | | |
| | | CCI0A | CCR0 | TA0 | |
| | Timer0_A3 CCR0B output (internal) | CCI0B | | | |
| | DVSS | GND | | | |
| | DVCC | VCC | | | |
| P4.0 | TA1.1 | CCI1A | CCR1 | TA1 | TA1.1 |
| | Timer0_A3 CCR1B output (internal) | CCI1B | | | to ADC trigger |
| | DVSS | GND | | | |
| | DVCC | VCC | | | |
| P8.3 | TA1.2 | CCI2A | CCR2 | TA2 | TA1.2 |
| | Timer0_A3 CCR2B output (internal) | CCI2B | | | IR Input |
| | DVSS | GND | | | |
| | DVCC | VCC | | | |

The interconnection of Timer0_A3 and Timer1_A3 can be used to modulate the eUSCI_A pin of UCA0TXD/UCA0SIMO in either ASK or FSK mode, with which a user can easily acquire a modulated infrared command for directly driving an external IR diode. The IR functions are fully controlled by SYS configuration registers 1 including IREN (enable), IRPSEL (polarity select), IRMSEL (mode select), IRDSEL (data select), and IRDATA (data) bits. For more information, refer to the SYS chapter in the *MSP430FR4xx and MSP430FR2xx Family User's Guide* ([SLAU445](#)).

6.9.9 Real-Time Clock counter (RTC)

The RTC counter is a 16-bit modulo counter that is functional in AM, LPM0, LPM3, and LPM3.5. This module may periodically wake up the CPU from LPM0, LPM3, and LPM3.5 based on timing from a low-power clock source such as the XT1 and VLO clocks. In AM, RTC can be driven by SMCLK to generate high-frequency timing events and interrupts. The RTC overflow events trigger:

- Timer0_A3 CCR1B
- ADC conversion trigger when ADCSHSx bits are set as 01b

6.9.10 10-Bit Analog Digital Converter (ADC)

The 10-bit ADC module supports fast 10-bit analog-to-digital conversions with single-ended input. The module implements a 10-bit SAR core, sample select control, reference generator and a conversion result buffer. A window comparator with a lower and upper limit allows CPU independent result monitoring with three window comparator interrupt flags.

The ADC supports 10 external inputs and four internal inputs (see [Table 6-12](#)).

Table 6-12. ADC Channel Connections

| ADC SHSx | ADC CHANNELS | EXTERNAL PIN OUT |
|----------|----------------------------|---------------------|
| 0 | A0/V _{ref-} | P1.0 |
| 1 | A1/V _{ref+} | P1.1 |
| 2 | A2 | P1.2 |
| 3 | A3 | P1.3 |
| 4 | A4 ⁽¹⁾ | P1.4 |
| 5 | A5 | P1.5 |
| 6 | A6 | P1.6 |
| 7 | A7 | P1.7 |
| 8 | A8 | P8.0 ⁽²⁾ |
| 9 | A9 | P8.1 ⁽²⁾ |
| 10 | Not Used | N/A |
| 11 | Not Used | N/A |
| 12 | On-chip Temperature Sensor | N/A |
| 13 | Reference Voltage (1.5 V) | N/A |
| 14 | DVSS | N/A |
| 15 | DVCC | N/A |

(1) When A4 is used, the PMM 1.2-V reference voltage can be output to this pin by setting the PMM control register. The 1.2-V voltage can be directly measured by A4 channel.

(2) P8.0 and P8.1 are only available in the LQFP-64 package.

The AD conversion can be started by software or a hardware trigger. [Table 6-13](#) shows the trigger sources that are available.

Table 6-13. ADC Trigger Signal Connections

| ADC SHSx | | TRIGGER SOURCE |
|----------|---------|------------------------------|
| Binary | Decimal | |
| 00 | 0 | ADCSC bit (software trigger) |
| 01 | 1 | RTC event |
| 10 | 2 | TA1.1B |
| 11 | 3 | TA1.2B |

6.9.11 Liquid Crystal Display (LCD)

The LCD driver generates the segment and common signals to drive segment liquid crystal display (LCD) glass. The LCD controller has dedicated data memories to hold segment drive information. Common and segment signals are generated as defined by the mode. Static, 2-mux, 3-mux, up to 8-mux LCDs are supported. The module can provide an LCD voltage independent from the main supply voltage with its integrated charge pump. The LCD display contrast can be trimmed by setting the LCD drive voltage. The LCD module can be fully functional in any power mode from AM to LPM3.5.

When supplied by the on-chip charge pump with on-chip regulator reference, the LCD driver needs five pins and four external 0.1- μ F capacitors to achieve low-power consumption during operation. [Figure 6-1](#) shows the recommended connections.

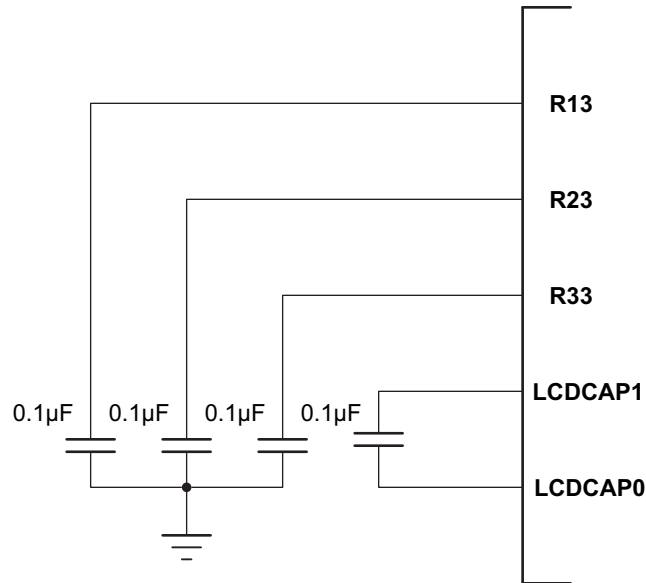


Figure 6-1. LCD Power Supply Configuration With On-Chip Charge Pump and Regulator Reference

The LCD contains 20 16-bit words (40 bytes) display memory. The use of memory is flexible, depending on the selected mode:

- 4-mux mode
 - LCDM0 to LCDM19 can be used for LCD display contents. If it is not used as LCD drive pin, the corresponding LCDMx can be used for user data (up to 20 bytes).
 - LCDBM0 to LCDBM19 can be used for LCD blinking contents. If it is not used as blinking, the corresponding LCDBMx can be used for user data (up to 20 bytes).
- 8-mux mode
 - LCDM0 to LCDM39 can be used for LCD display contents. If it is not used as LCD drive pin, the corresponding LCDMx can be used for user data (up to 40 bytes).

6.9.12 Embedded Emulation Module (EEM)

The EEM supports real-time in-system debugging. The EEM on these devices has the following features:

- Three hardware triggers or breakpoints on memory access
- One hardware trigger or breakpoint on CPU register write access
- Up to four hardware triggers can be combined to form complex triggers or breakpoints
- One cycle counter
- Clock control on module level

6.9.13 Input/Output Schematics

6.9.13.1 Port P1 Input/Output With Schmitt Trigger

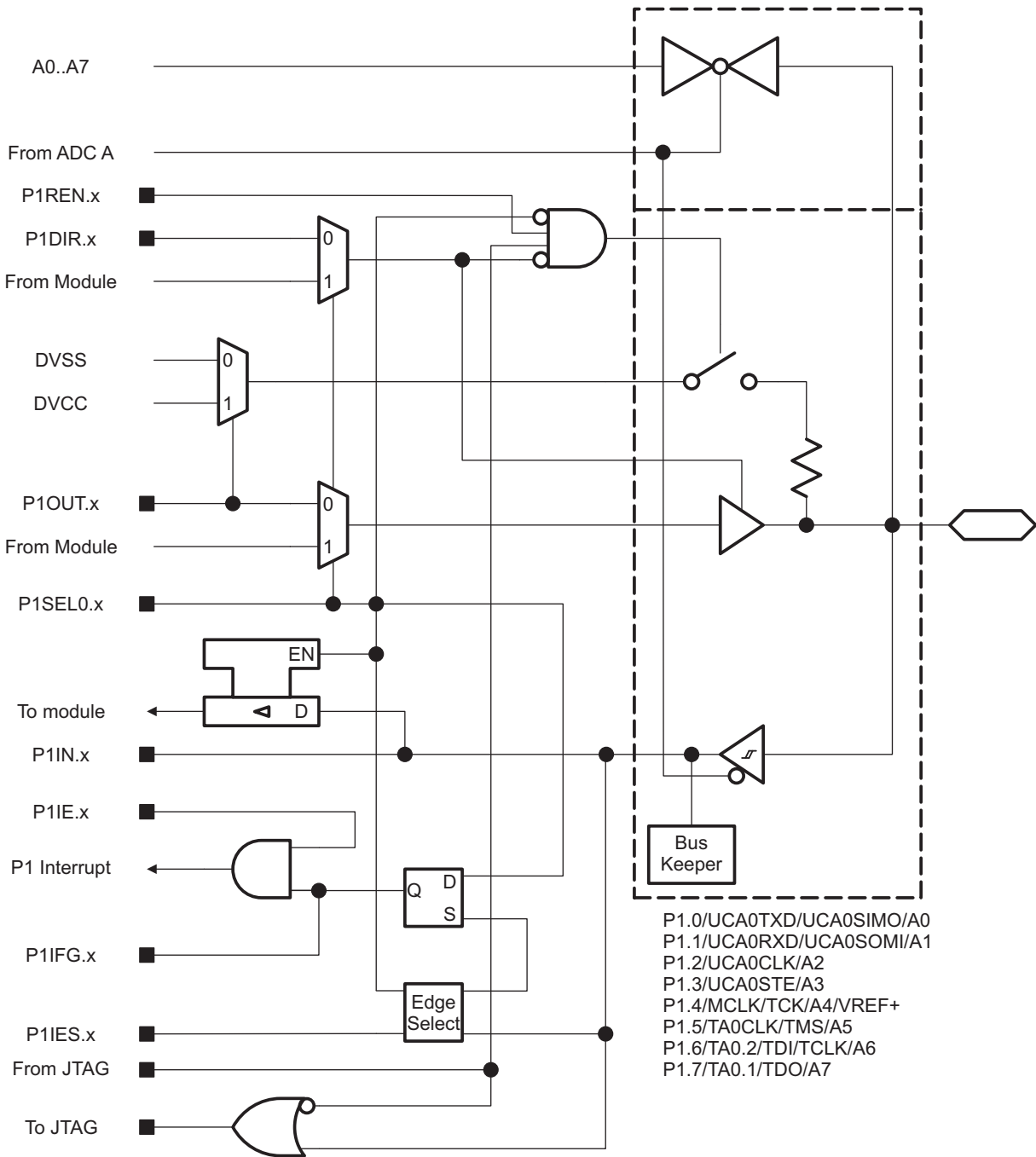


Figure 6-2. Port P1 Input/Output With Schmitt Trigger

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Table 6-14. Port P1 Pin Functions

| PIN NAME (P1.x) | x | FUNCTION | CONTROL BITS AND SIGNALS ⁽¹⁾ | | | |
|------------------------------|---|------------------|---|----------|-------------------------|----------|
| | | | P1DIR.x | P1SEL0.x | ADCPCTLx ⁽²⁾ | JTAG |
| P1.0/UCA0TXD/ UCA0SIMO/A0 | 0 | P1.0 (I/O) | I: 0; O: 1 | 0 | 0 | N/A |
| | | UCA0TXD/UCA0SIMO | X | 1 | 0 | N/A |
| | | A0 | X | X | 1 (x = 0) | N/A |
| P1.1/UCA0RXD/ UCA0SOMI/A1 | 1 | P1.1 (I/O) | I: 0; O: 1 | 0 | 0 | N/A |
| | | UCA0RXD/UCA0SOMI | X | 1 | 0 | N/A |
| | | A1 | X | X | 1 (x = 1) | N/A |
| P1.2/UCA0CLK/A2 | 2 | P1.2 (I/O) | I: 0; O: 1 | 0 | 0 | N/A |
| | | UCA0CLK | X | 1 | 0 | N/A |
| | | A2 | X | X | 1 (x = 2) | N/A |
| P1.3/UCA0STE/A3 | 3 | P1.3 (I/O) | I: 0; O: 1 | 0 | 0 | N/A |
| | | UCA0STE | X | 1 | 0 | N/A |
| | | A3 | X | X | 1 (x = 3) | N/A |
| P1.4/MCLK/TCK/A4/ VREF+ | 4 | P1.4 (I/O) | I: 0; O: 1 | 0 | 0 | Disabled |
| | | VSS | 0 | 1 | 0 | Disabled |
| | | MCLK | 1 | | | |
| | | A4, VREF+ | X | X | 1 (x = 4) | Disabled |
| | | JTAG TCK | X | X | X | TCK |
| P1.5/TA0CLK/TMS/A5 | 5 | P1.5 (I/O) | I: 0; O: 1 | 0 | 0 | Disabled |
| | | TA0CLK | 0 | 1 | 0 | Disabled |
| | | VSS | 1 | | | |
| | | A5 | X | X | 1 (x = 5) | Disabled |
| | | JTAG TMS | X | X | X | TMS |
| P1.6/TA0.2/TDI/TCLK/ A6 | 6 | P1.6 (I/O) | I: 0; O: 1 | 0 | 0 | Disabled |
| | | TA0.CCI2A | 0 | 1 | 0 | Disabled |
| | | TA0.2 | 1 | | | |
| | | A6 | X | X | 1 (x = 6) | Disabled |
| | | JTAG TDI/TCLK | X | X | X | TDI/TCLK |
| P1.7/TA0.1/TDO/A7 | 7 | P1.7 (I/O) | I: 0; O: 1 | 0 | 0 | Disabled |
| | | TA0.CCI1A | 0 | 1 | 0 | Disabled |
| | | TA0.1 | 1 | | | |
| | | A7 | X | X | 1 (x = 7) | Disabled |
| | | JTAG TDO | X | X | X | TDO |

(1) X = don't care

(2) Setting the ADCPCTLx bit in SYSCFG2 register will disable both the output driver and input Schmitt trigger to prevent leakage when analog signals are applied.

6.9.13.2 Port P2 Input/Output With Schmitt Trigger

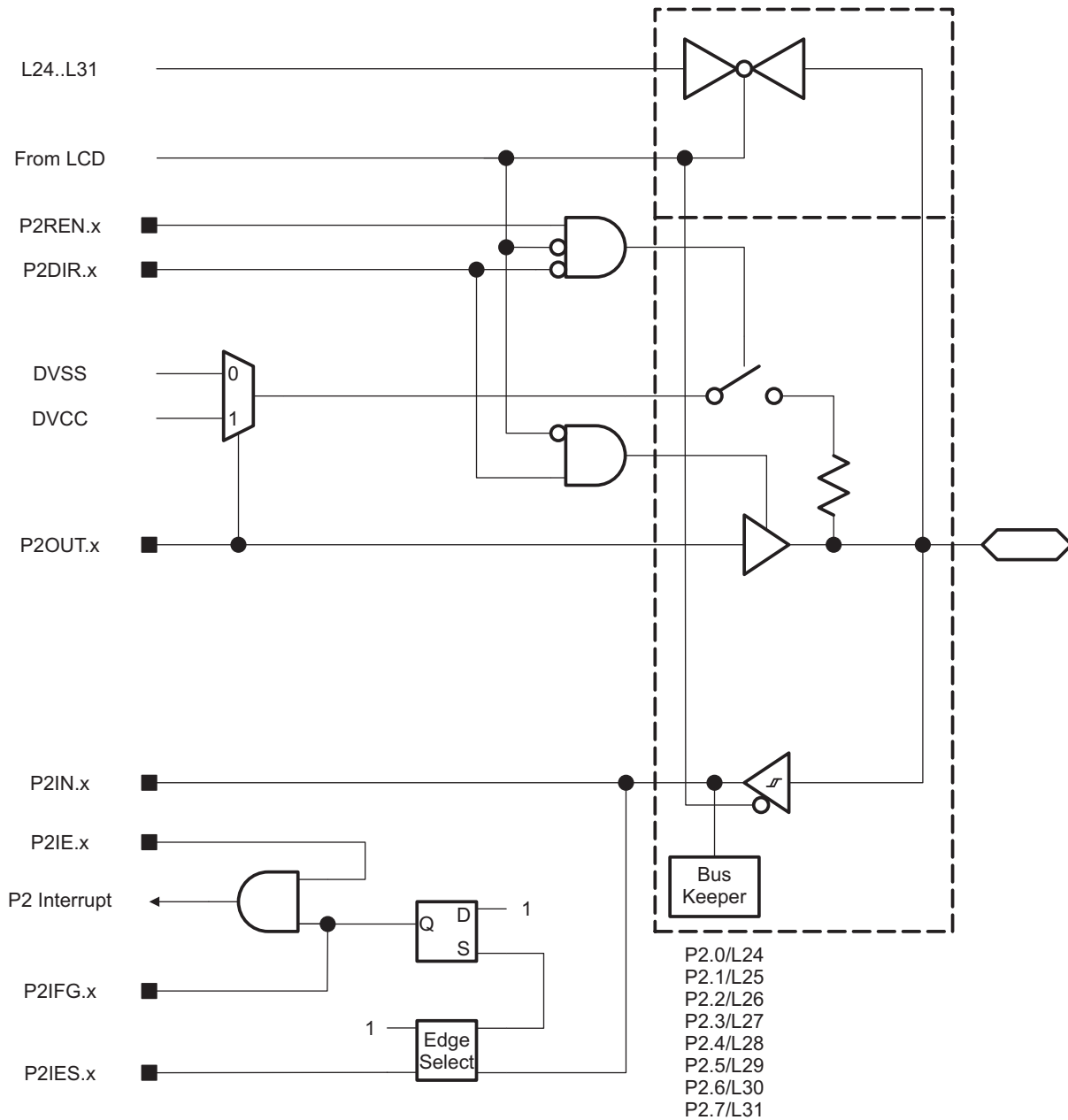


Figure 6-3. Port P2 Input/Output With Schmitt Trigger

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Table 6-15. Port P2 Pin Functions

| PIN NAME (P2.x) | x | FUNCTION | CONTROL BITS AND SIGNALS ⁽¹⁾ | |
|-----------------|---|------------|---|------------|
| | | | P2DIR.x | LCDSy |
| P2.0/L24 | 0 | P2.0 (I/O) | I: 0; O: 1 | 0 |
| | | L24 | X | 1 (y = 24) |
| P2.1/L25 | 1 | P2.1 (I/O) | I: 0; O: 1 | 0 |
| | | L25 | X | 1 (y = 25) |
| P2.2/L26 | 2 | P2.2 (I/O) | I: 0; O: 1 | 0 |
| | | L26 | X | 1 (y = 26) |
| P2.3/L27 | 3 | P2.3 (I/O) | I: 0; O: 1 | 0 |
| | | L27 | X | 1 (y = 27) |
| P2.4/L28 | 4 | P2.4 (I/O) | I: 0; O: 1 | 0 |
| | | L28 | X | 1 (y = 28) |
| P2.5/L29 | 5 | P2.5 (I/O) | I: 0; O: 1 | 0 |
| | | L29 | X | 1 (y = 29) |
| P2.6/L30 | 6 | P2.6 (I/O) | I: 0; O: 1 | 0 |
| | | L30 | X | 1 (y = 30) |
| P2.7/L31 | 7 | P2.7 (I/O) | I: 0; O: 1 | 0 |
| | | L31 | X | 1 (y = 31) |

(1) X = don't care

6.9.13.3 Port P3 Input/Output With Schmitt Trigger

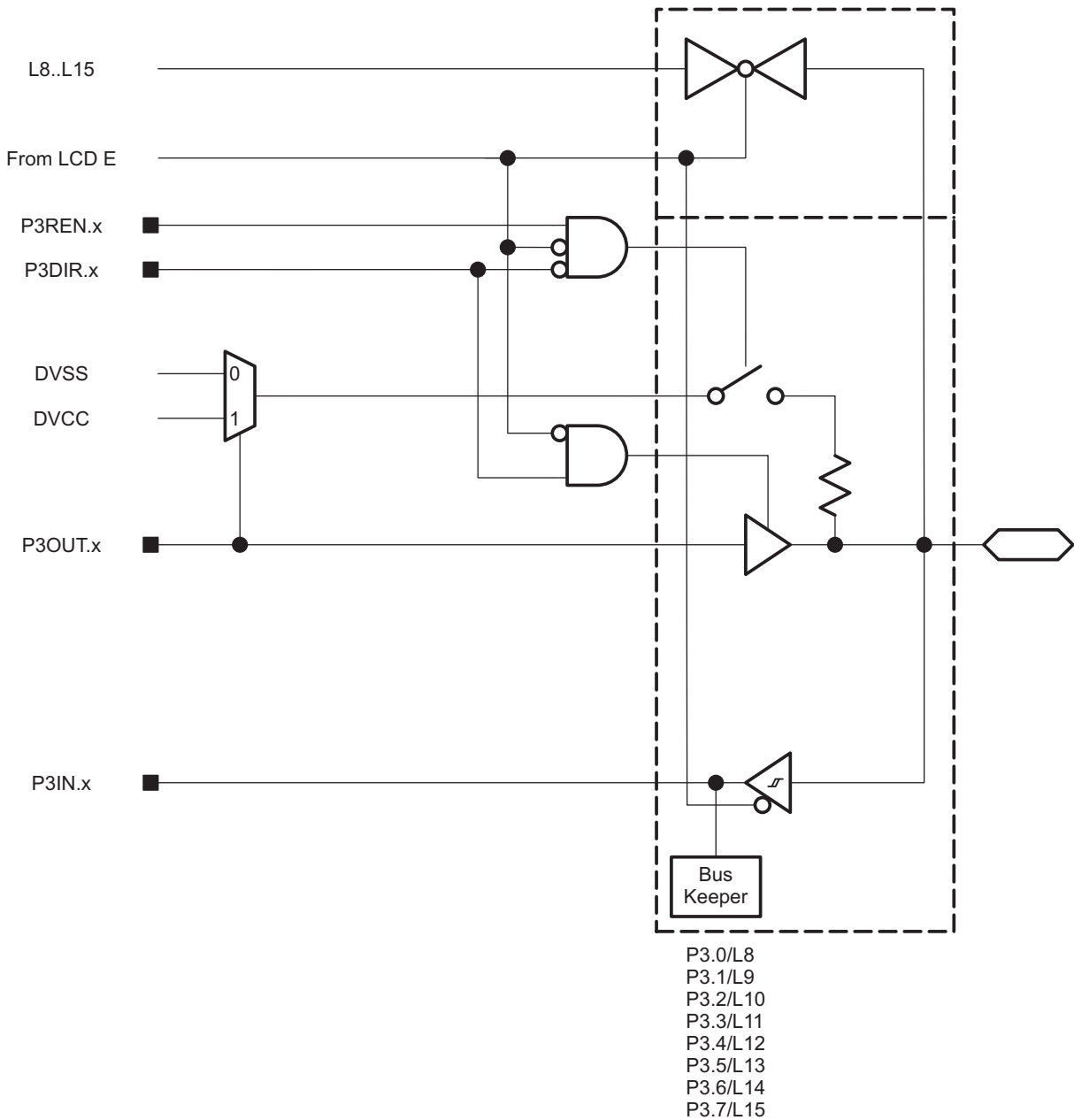


Figure 6-4. Port P3 Input/Output With Schmitt Trigger

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Table 6-16. Port P3 Pin Functions

| PIN NAME (P3.x) | x | FUNCTION | CONTROL BITS AND SIGNALS ⁽¹⁾ | |
|-----------------|---|------------|---|------------|
| | | | P3DIR.x | LCDSy |
| P3.0/L8 | 0 | P3.0 (I/O) | I: 0; O: 1 | 0 |
| | | L8 | X | 1 (y = 8) |
| P3.1/L9 | 1 | P3.1 (I/O) | I: 0; O: 1 | 0 |
| | | L9 | X | 1 (y = 9) |
| P3.2/L10 | 2 | P3.2 (I/O) | I: 0; O: 1 | 0 |
| | | L10 | X | 1 (y = 10) |
| P3.3/L11 | 3 | P3.3 (I/O) | I: 0; O: 1 | 0 |
| | | L11 | X | 1 (y = 11) |
| P3.4/L12 | 4 | P3.4 (I/O) | I: 0; O: 1 | 0 |
| | | L12 | X | 1 (y = 12) |
| P3.5/L13 | 5 | P3.5 (I/O) | I: 0; O: 1 | 0 |
| | | L13 | X | 1 (y = 13) |
| P3.6/L14 | 6 | P3.6 (I/O) | I: 0; O: 1 | 0 |
| | | L14 | X | 1 (y = 14) |
| P3.7/L15 | 7 | P3.7 (I/O) | I: 0; O: 1 | 0 |
| | | L15 | X | 1 (y = 15) |

(1) X = don't care

6.9.13.4 Port P4.0 Input/Output With Schmitt Trigger

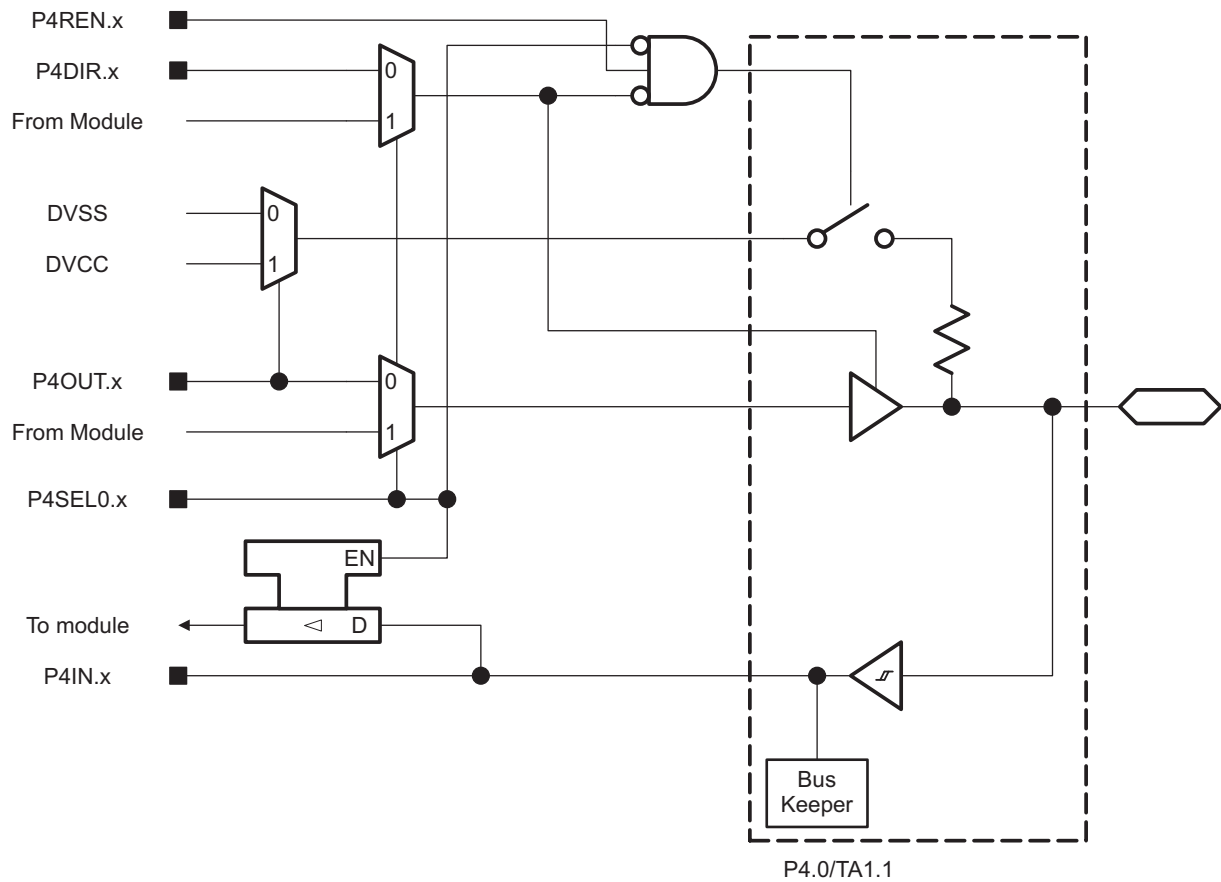


Figure 6-5. Port P4.0 Input/Output With Schmitt Trigger

Table 6-17. Port P4.0 Pin Functions

| PIN NAME (P4.x) | x | FUNCTION | CONTROL BITS AND SIGNALS | |
|-----------------|---|------------|--------------------------|----------|
| | | | P4DIR.x | P4SEL0.x |
| P4.0/TA1.1 | 0 | P4.0 (I/O) | I: 0; O: 1 | 0 |
| | | TA1.CCI1A | 0 | 1 |
| | | TA1.1 | 1 | |

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6.9.13.5 Port P4.1 and P4.2 Input/Output With Schmitt Trigger

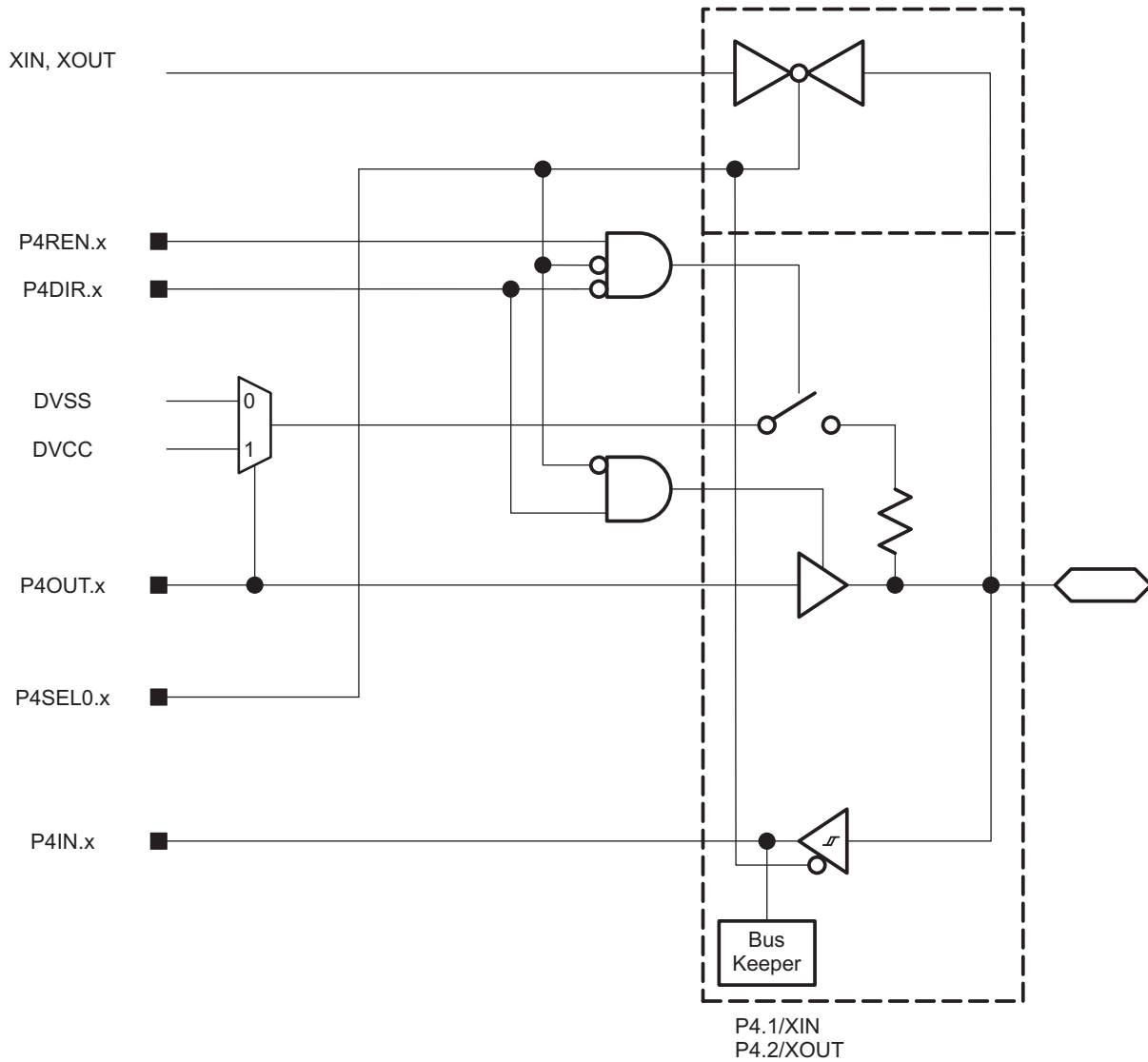


Figure 6-6. Port P4.1 and P4.2 Input/Output With Schmitt Trigger

Table 6-18. Port P4.1 and P4.2 Pin Functions

| PIN NAME (P4.x) | x | FUNCTION | CONTROL BITS AND SIGNALS ⁽¹⁾ | |
|-----------------|---|------------|---|----------|
| | | | P4DIR.x | P4SEL0.x |
| P4.1/XIN | 1 | P4.1 (I/O) | I: 0; O: 1 | 0 |
| | | XIN | X | 1 |
| P4.2/XOUT | 2 | P4.2 (I/O) | I: 0; O: 1 | 0 |
| | | XOUT | X | 1 |

(1) X = don't care

6.9.13.6 Port 4.3, P4.4, P4.5, P4.6, and P4.7 Input/Output With Schmitt Trigger

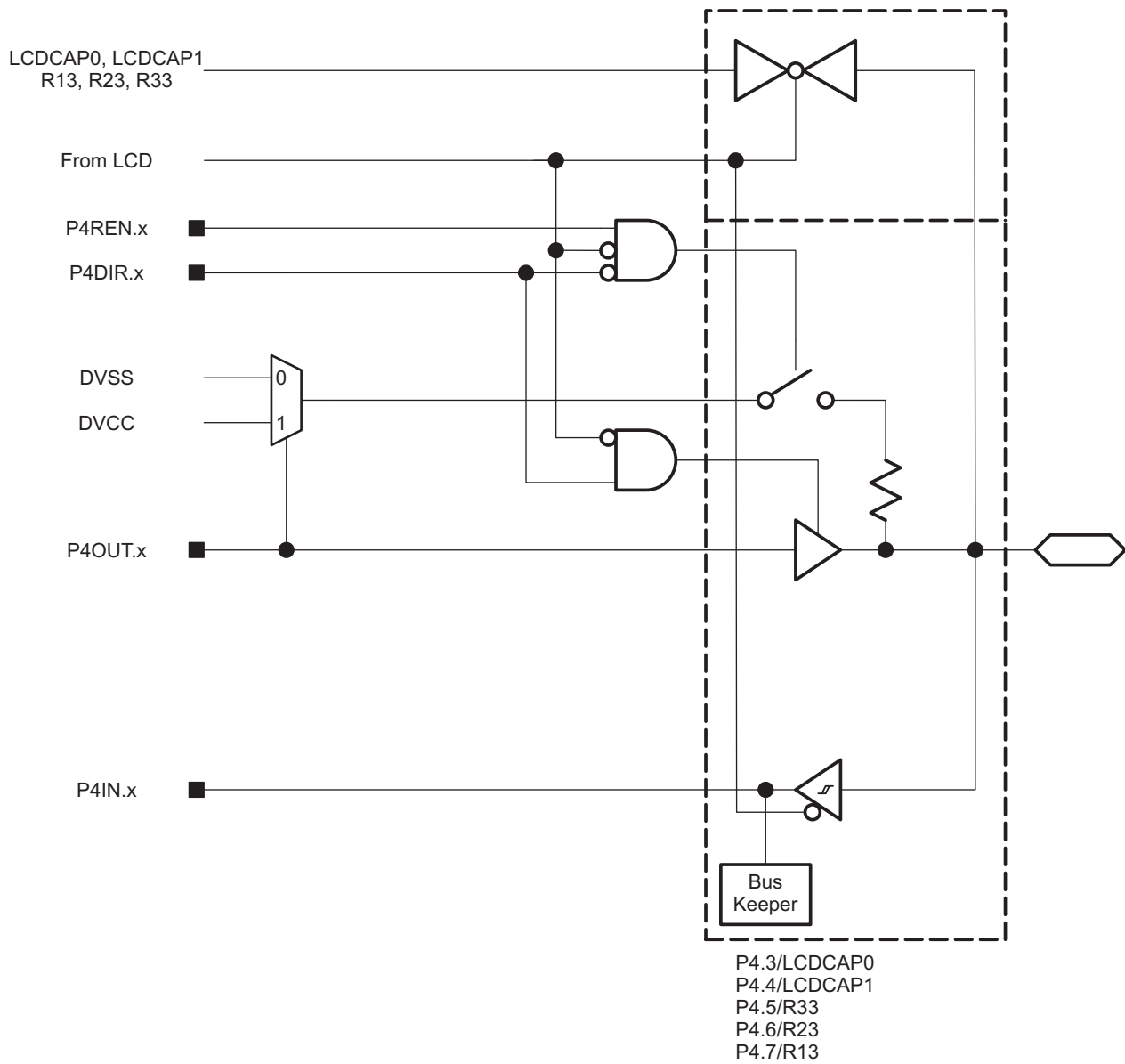


Figure 6-7. Port 4.3, P4.4, P4.5, P4.6, and P4.7 Input/Output With Schmitt Trigger

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Table 6-19. Port P4.3, P4.4, P4.5, P4.6, and P4.7 Pin Functions

| PIN NAME (P4.x) | x | FUNCTION | CONTROL BITS AND SIGNALS ⁽¹⁾ | |
|-----------------|---|------------|---|------------------------|
| | | | P4DIR.x | LCDPCTL ⁽²⁾ |
| P4.3/LCDCAP0 | 3 | P4.3 (I/O) | I: 0; O: 1 | X |
| | | LCDCAP0 | X | 1 |
| P4.4/LCDCAP1 | 4 | P4.4 (I/O) | I: 0; O: 1 | 0 |
| | | LCDCAP1 | X | 1 |
| P4.5/R33 | 5 | P4.5 (I/O) | I: 0; O: 1 | 0 |
| | | R33 | X | 1 |
| P4.6/R23 | 6 | P4.6 (I/O) | I: 0; O: 1 | 0 |
| | | R23 | X | 1 |
| P4.7/R13 | 7 | P4.7 (I/O) | I: 0; O: 1 | 0 |
| | | R13 | X | 1 |

(1) X = don't care

(2) Setting the LCDPCTL bit in SYSCFG2 register will disable both the output driver and input Schmitt trigger to prevent leakage when analog signals are applied.

6.9.13.7 Port P5.0, P5.1, P5.2, and P5.3 Input/Output With Schmitt Trigger

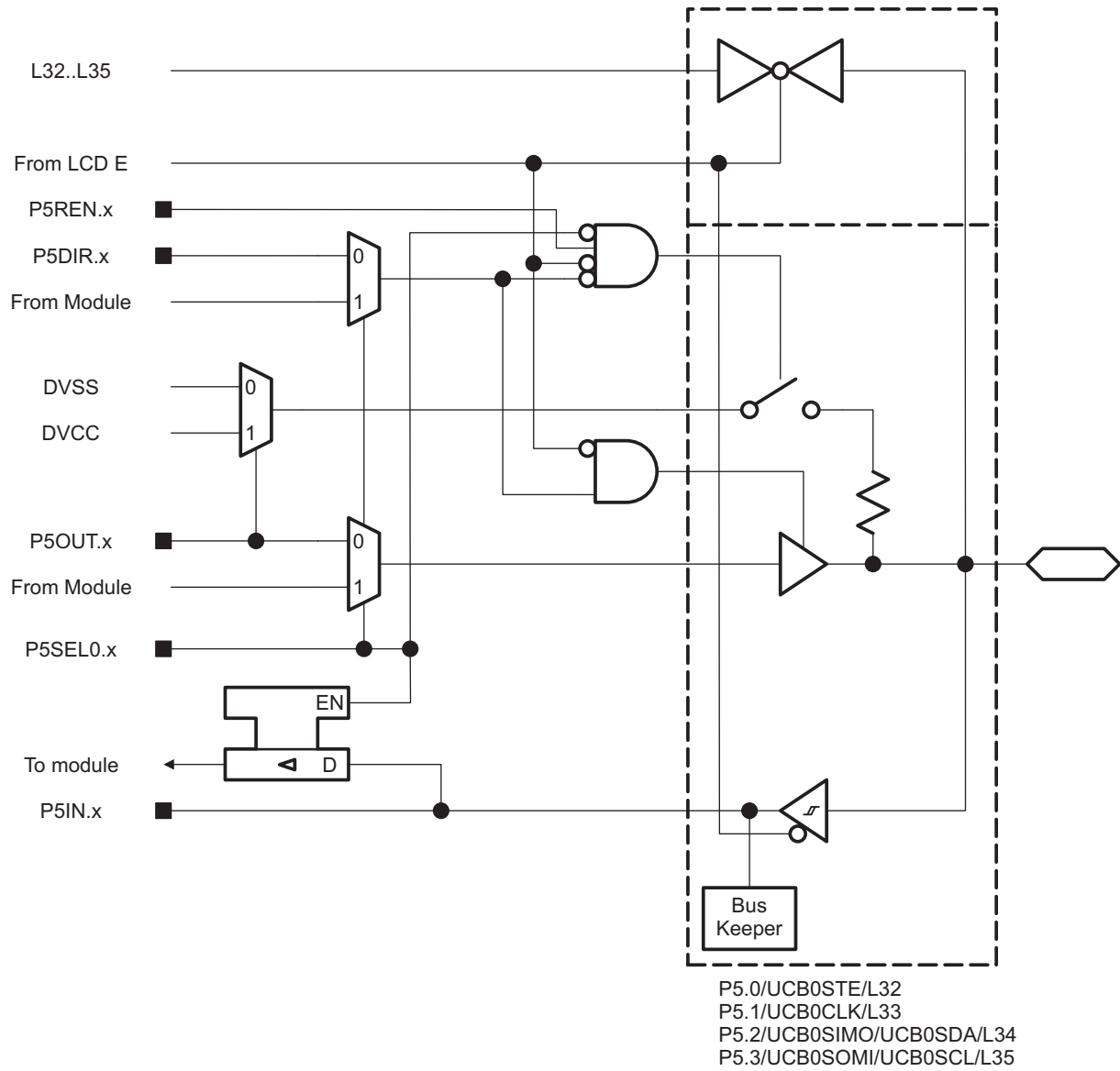


Figure 6-8. Port P5.0, P5.1, P5.2, and P5.3 Input/Output With Schmitt Trigger

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Table 6-20. Port P5.0, P5.1, P5.2, and P5.3 Pin Functions

| PIN NAME (P5.x) | x | FUNCTION | CONTROL BITS AND SIGNALS ⁽¹⁾ | | |
|-------------------------------|---|------------------|---|----------|------------|
| | | | P5DIR.x | P5SEL0.x | LCDSy |
| P5.0/UCB0STE/L32 | 0 | P5.0 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | UCB0STE | 0 | 1 | 0 |
| | | L32 | X | X | 1 (y = 32) |
| P5.1/UCB0CLK/L33 | 1 | P5.1 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | UCB0CLK | 0 | 1 | 0 |
| | | L33 | X | X | 1 (y = 33) |
| P5.2/UCB0SIMO/ UCB0SDA/L34 | 2 | P5.2 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | UCB0SIMO/UCB0SDA | 0 | 1 | 0 |
| | | L34 | X | X | 1 (y = 34) |
| P5.3/UCB0SOMI/ UCB0SCL/L35 | 3 | P5.3 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | UCB0SOMI/UCB0SCL | 0 | 1 | 0 |
| | | L35 | X | X | 1 (y = 35) |

(1) X = don't care

6.9.13.8 Port P5.4, P5.5, P5.6, and P5.7 Input/Output With Schmitt Trigger

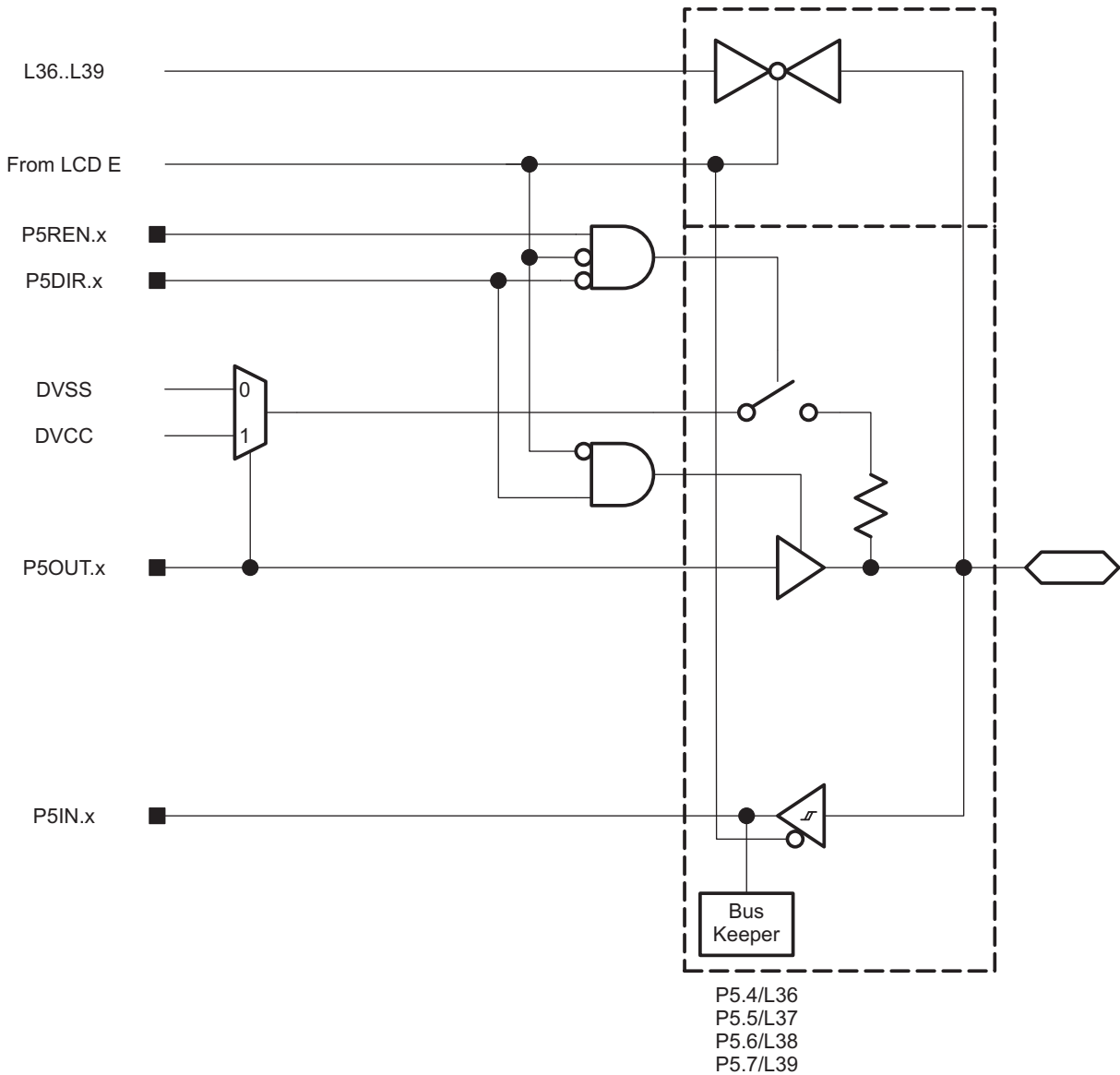


Figure 6-9. Port P5.4, P5.5, P5.6, and P5.7 Input/Output With Schmitt Trigger

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Table 6-21. Port P5.4, P5.5, P5.6, and P5.7 Pin Functions

| PIN NAME (P5.x) | x | FUNCTION | CONTROL BITS AND SIGNALS ⁽¹⁾ | |
|-----------------|---|------------|---|------------|
| | | | P5DIR.x | LCDSy |
| P5.4/L36 | 4 | P5.4 (I/O) | I: 0; O: 1 | 0 |
| | | L36 | X | 1 (y = 36) |
| P5.5/L37 | 5 | P5.5 (I/O) | I: 0; O: 1 | 0 |
| | | L37 | X | 1 (y = 37) |
| P5.6/L38 | 6 | P5.6 (I/O) | I: 0; O: 1 | 0 |
| | | L38 | X | 1 (y = 38) |
| P5.7/L39 | 7 | P5.7 (I/O) | I: 0; O: 1 | 0 |
| | | L39 | X | 1 (y = 39) |

(1) X = don't care

6.9.13.9 Port P6 Input/Output With Schmitt Trigger

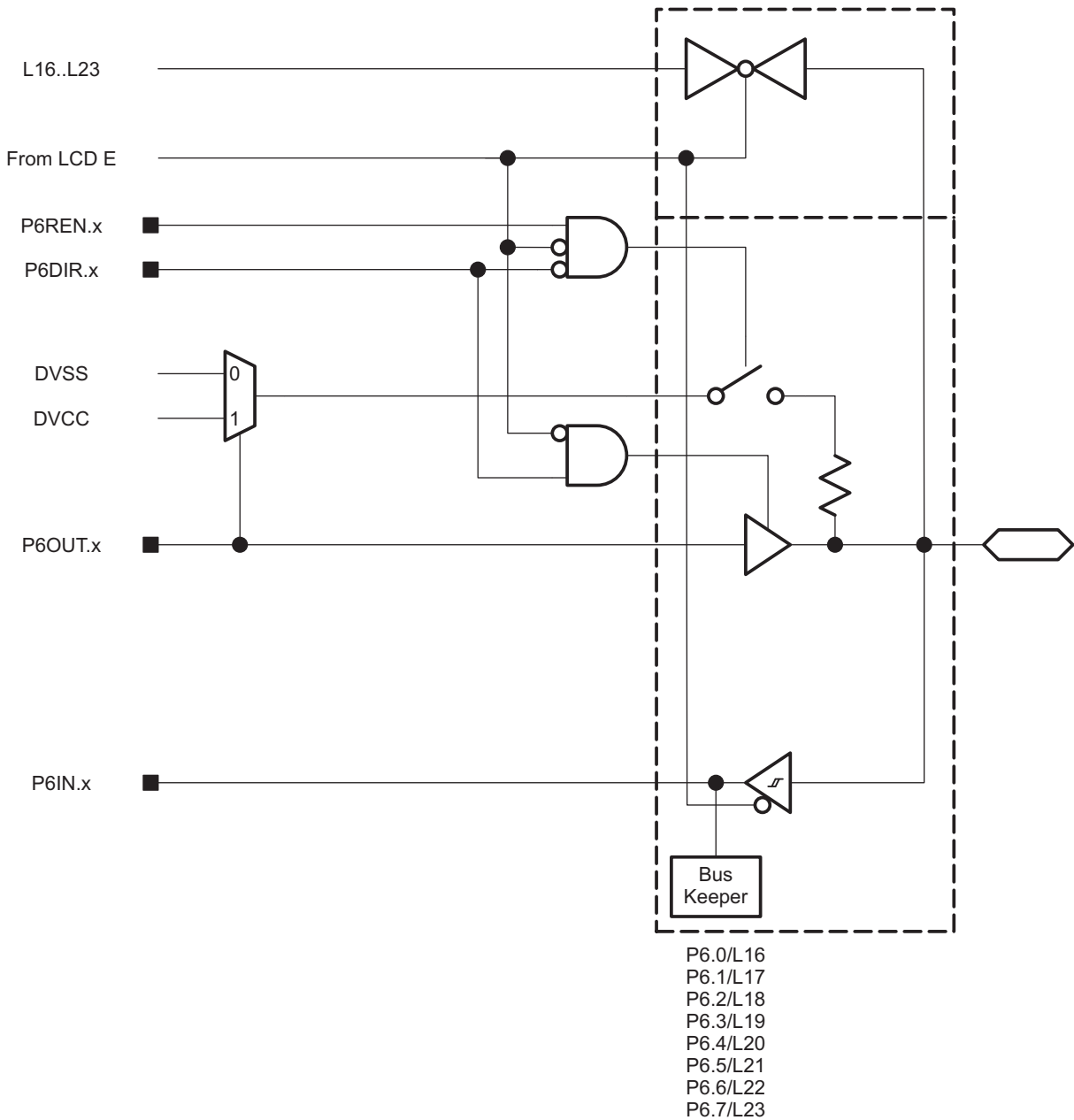


Figure 6-10. Port P6 Input/Output With Schmitt Trigger

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Table 6-22. Port P6 Pin Functions

| PIN NAME (P6.x) | x | FUNCTION | CONTROL BITS AND SIGNALS ⁽¹⁾ | |
|-----------------|---|------------|---|------------|
| | | | P6DIR.x | LCDSy |
| P6.0/L16 | 0 | P6.0 (I/O) | I: 0; O: 1 | 0 |
| | | L16 | X | 1 (y = 16) |
| P6.1/L17 | 1 | P6.1 (I/O) | I: 0; O: 1 | 0 |
| | | L17 | X | 1 (y = 17) |
| P6.2/L18 | 2 | P6.2 (I/O) | I: 0; O: 1 | 0 |
| | | L18 | X | 1 (y = 18) |
| P6.3/L19 | 3 | P6.3 (I/O) | I: 0; O: 1 | 0 |
| | | L19 | X | 1 (y = 19) |
| P6.4/L20 | 4 | P6.4 (I/O) | I: 0; O: 1 | 0 |
| | | L20 | X | 1 (y = 20) |
| P6.5/L21 | 5 | P6.5 (I/O) | I: 0; O: 1 | 0 |
| | | L21 | X | 1 (y = 21) |
| P6.6/L22 | 6 | P6.6 (I/O) | I: 0; O: 1 | 0 |
| | | L22 | X | 1 (y = 22) |
| P6.7/L23 | 7 | P6.7 (I/O) | I: 0; O: 1 | 0 |
| | | L23 | X | 1 (y = 23) |

(1) X = don't care

6.9.13.10 Port P7 Input/Output With Schmitt Trigger

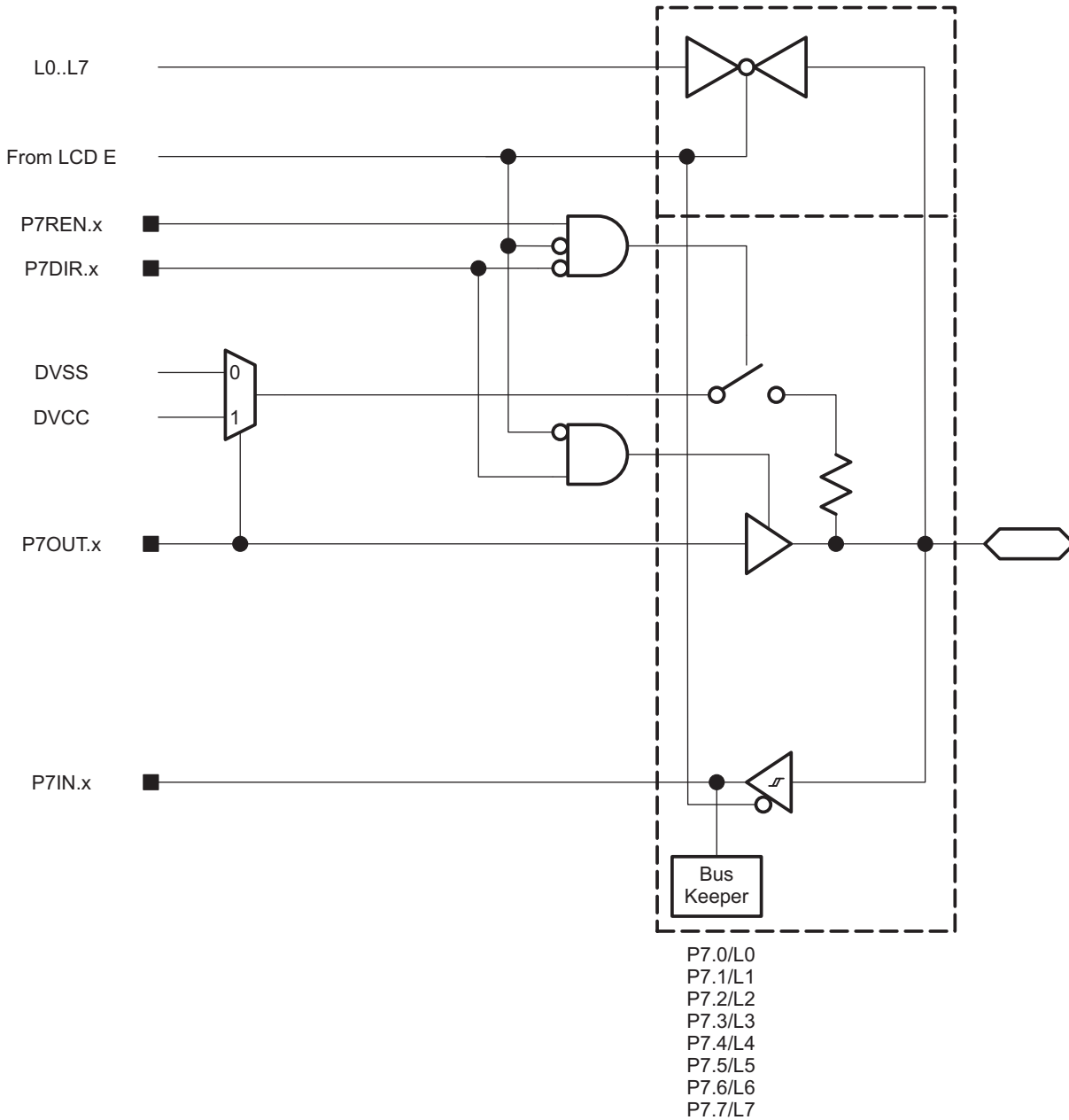


Figure 6-11. Port P7 Input/Output With Schmitt Trigger

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Table 6-23. Port P7 Pin Functions

| PIN NAME (P7.x) | x | FUNCTION | CONTROL BITS AND SIGNALS ⁽¹⁾ | |
|-----------------|---|------------|---|-----------|
| | | | P7DIR.x | LCDSy |
| P7.0/L0 | 0 | P7.0 (I/O) | I: 0; O: 1 | 0 |
| | | L0 | X | 1 (y = 0) |
| P7.1/L1 | 1 | P7.1 (I/O) | I: 0; O: 1 | 0 |
| | | L1 | X | 1 (y = 1) |
| P7.2/L2 | 2 | P7.2 (I/O) | I: 0; O: 1 | 0 |
| | | L2 | X | 1 (y = 2) |
| P7.3/L3 | 3 | P7.3 (I/O) | I: 0; O: 1 | 0 |
| | | L3 | X | 1 (y = 3) |
| P7.4/L4 | 4 | P7.4 (I/O) | I: 0; O: 1 | 0 |
| | | L4 | X | 1 (y = 4) |
| P7.5/L5 | 5 | P7.5 (I/O) | I: 0; O: 1 | 0 |
| | | L5 | X | 1 (y = 5) |
| P7.6/L6 | 6 | P7.6 (I/O) | I: 0; O: 1 | 0 |
| | | L6 | X | 1 (y = 6) |
| P7.7/L7 | 7 | P7.7 (I/O) | I: 0; O: 1 | 0 |
| | | L7 | X | 1 (y = 7) |

(1) X = don't care

6.9.13.11 Port P8.0 and P8.1 Input/Output With Schmitt Trigger

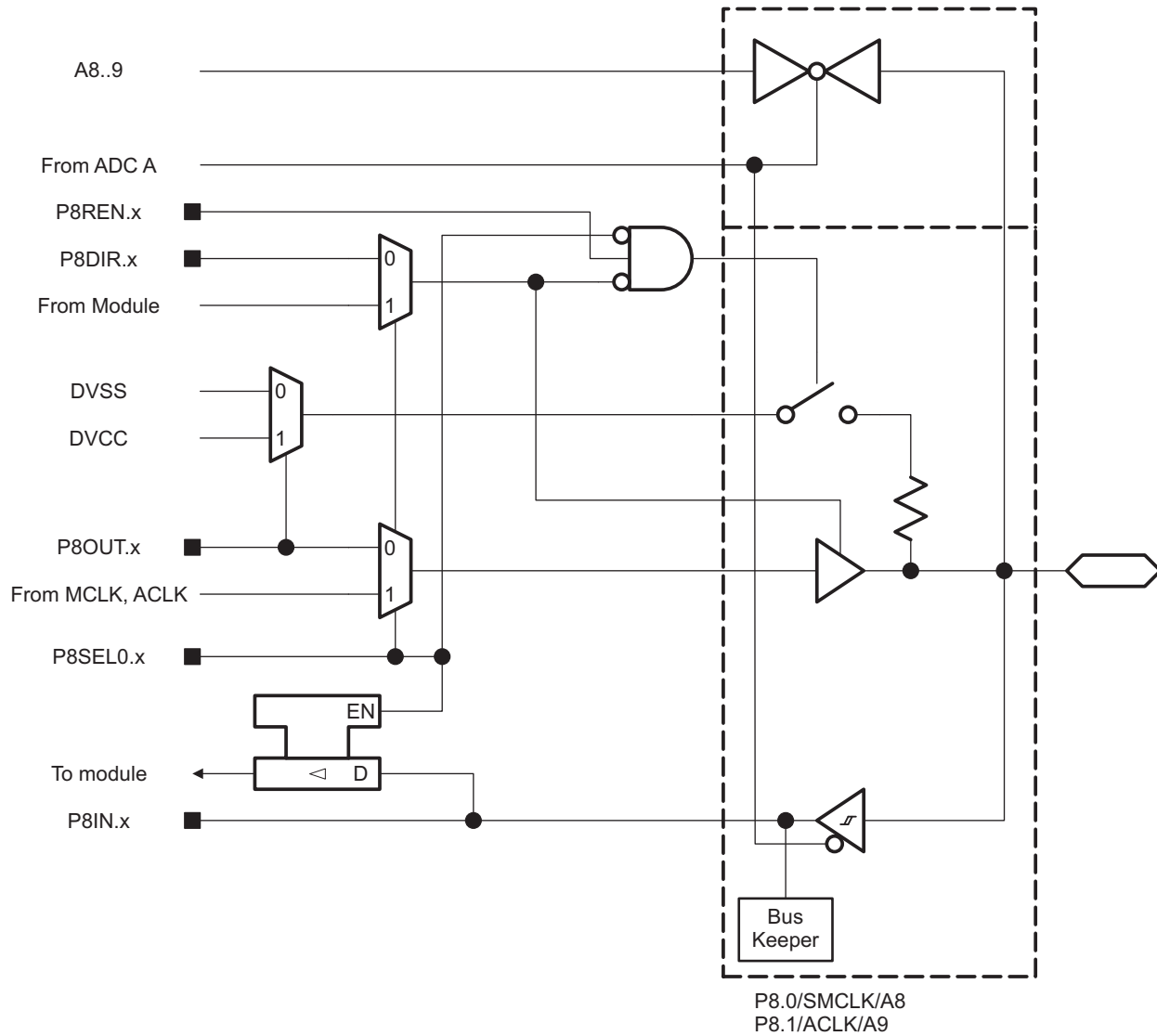


Figure 6-12. Port P8.0 and P8.1 Input/Output With Schmitt Trigger

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Table 6-24. Port P8.0 and P8.1 Pin Functions

| PIN NAME (P8.x) | x | FUNCTION | CONTROL BITS AND SIGNALS ⁽¹⁾ | | |
|-----------------|---|------------|---|----------|-------------------------|
| | | | P8DIR.x | P8SEL0.x | ADCPCTLx ⁽²⁾ |
| P8.0/SMCLK/A8 | 0 | P8.0 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | VSS | 0 | 1 | 0 |
| | | SMCLK | 1 | | |
| | | A8 | X | X | 1 (x = 8) |
| P8.1/ACLK/A9 | 1 | P8.1 (I/O) | I: 0; O: 1 | 0 | 0 |
| | | VSS | 0 | 1 | 0 |
| | | ACLK | 1 | | |
| | | A9 | X | X | 1 (x = 9) |

(1) X = don't care

(2) Setting the ADCPCTLx bit in SYSCFG2 register will disable both the output driver and input Schmitt trigger to prevent leakage when analog signals are applied.

6.9.13.12 Port P8.2 and P8.3 Input/Output With Schmitt Trigger

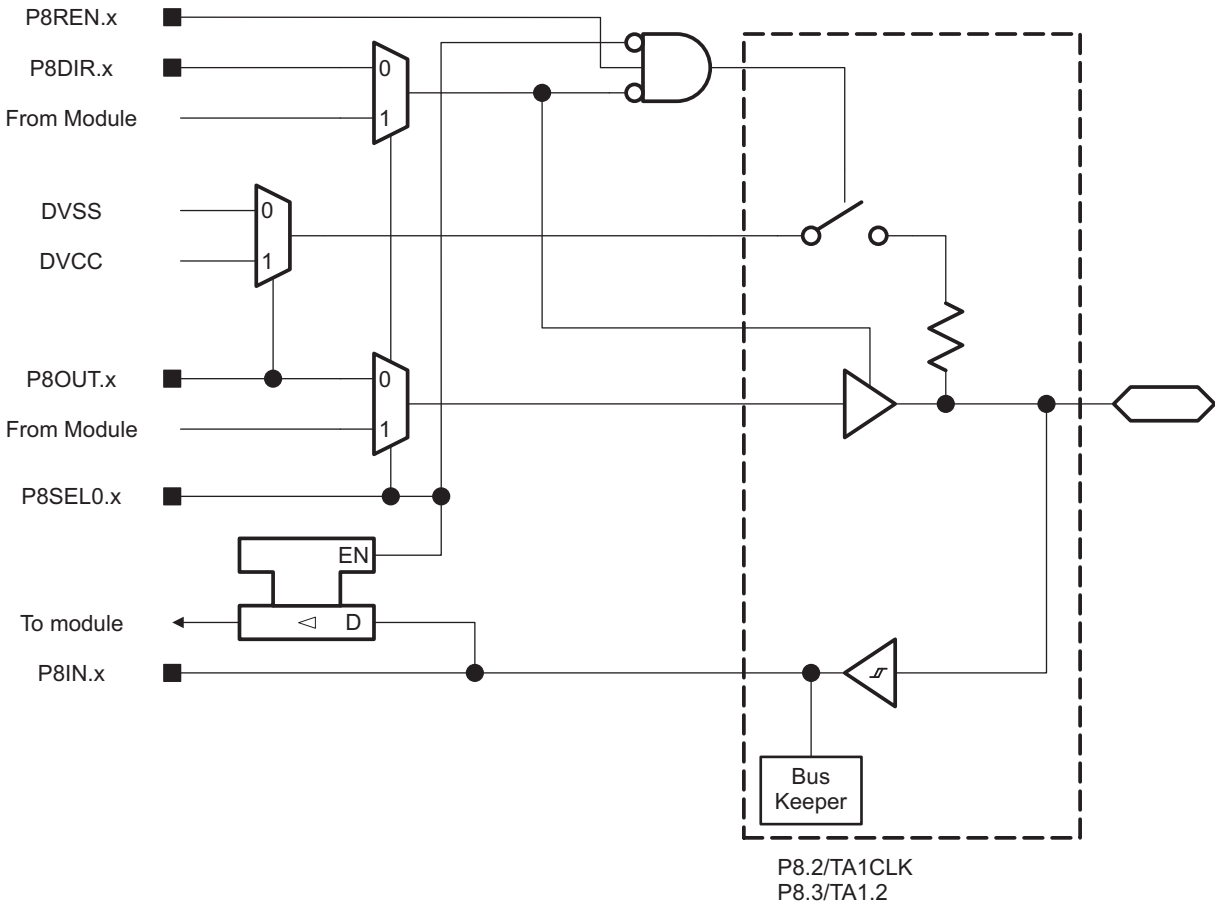


Figure 6-13. Port P8.2 and P8.3 Input/Output With Schmitt Trigger

Table 6-25. Port P8.2 and P8.3 Pin Functions

| PIN NAME (P8.x) | x | FUNCTION | CONTROL BITS AND SIGNALS | |
|-----------------|---|------------|--------------------------|----------|
| | | | P8DIR.x | P8SEL0.x |
| P8.2/TA1CLK | 2 | P8.2 (I/O) | I: 0; O: 1 | 0 |
| | | TA1 CLK | 0 | 1 |
| | | VSS | 1 | 1 |
| P8.3/TA1.2 | 3 | P8.3 (I/O) | I: 0; O: 1 | 0 |
| | | TA1.CCI2A | 0 | 1 |
| | | TA1.2 | 1 | |

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6.10 Device Descriptors (TLV)

Table 6-26 lists the Device IDs of the MSP430FR413x device variants. Table 6-27 lists the contents of the device descriptor tag-length-value (TLV) structure for MSP430FR413x devices.

Table 6-26. Device IDs

| DEVICE | DEVICE ID | |
|--------------|-----------|-------|
| | 1A04h | 1A05h |
| MSP430FR4133 | F0h | 81h |
| MSP430FR4132 | F1h | 81h |
| MSP430FR4131 | F2h | 81h |

Table 6-27. Device Descriptors

| | DESCRIPTION | MSP430FR413x | |
|--------------------------------------|--|--------------|----------------|
| | | ADDRESS | VALUE |
| Information Block | Info length | 1A00h | 06h |
| | CRC length | 1A01h | 06h |
| | CRC value | 1A02h | per unit |
| | | 1A03h | per unit |
| | Device ID | 1A04h | See Table 6-26 |
| | | 1A05h | |
| | Hardware revision | 1A06h | per unit |
| Firmware revision | 1A07h | per unit | |
| Die Record | Die Record Tag | 1A08h | 08h |
| | Die Record length | 1A09h | 0Ah |
| | Lot Wafer ID | 1A0Ah | per unit |
| | | 1A0Bh | per unit |
| | | 1A0Ch | per unit |
| | | 1A0Dh | per unit |
| | Die X position | 1A0Eh | per unit |
| | | 1A0Fh | per unit |
| | Die Y position | 1A10h | per unit |
| | | 1A11h | per unit |
| Test Result | 1A12h | per unit | |
| | 1A13h | per unit | |
| ADC Calibration | ADC Calibration Tag | 1A14h | per unit |
| | ADC Calibration Length | 1A15h | per unit |
| | ADC Gain Factor | 1A16h | per unit |
| | | 1A17h | per unit |
| | ADC Offset | 1A18h | per unit |
| | | 1A19h | per unit |
| | ADC 1.5-V Reference Temperature 30°C | 1A1Ah | per unit |
| | | 1A1Bh | per unit |
| ADC 1.5-V Reference Temperature 85°C | 1A1Ch | per unit | |
| | 1A1Dh | per unit | |
| DCO Calibration | DCO Tap Settings for 16 MHz, Temperature 30°C ⁽¹⁾ | 1A22h | per unit |
| | | 1A23h | perunit |

(1) This value can be directly loaded into DCO bits in CSCTL0 register to get accurate 16-MHz frequency at room temperature, especially when MCU exits from LPM3 and below. It is also suggested to use pre-divider to decrease the frequency, if the temperature drift might result an overshoot beyond 16 MHz.

6.11 Memory

Table 6-28 shows the memory organization of the MSP430FR413x devices.

Table 6-28. Memory Organization

| | ACCESS | MSP430FR4133 | MSP430FR4132 | MSP430FR4131 |
|--|---|-------------------------------------|------------------------------------|------------------------------------|
| Memory (FRAM) Main: interrupt vectors and signatures Main: code memory | Read/Write (Optional Write Protect) ⁽¹⁾ | 15 KB FFFFh-FF80h FFFFh-C400h | 8 KB FFFFh-FF80h FFFFh-E000h | 4 KB FFFFh-FF80h FFFFh-F000h |
| RAM | Read/Write | 2 KB 27FFh-2000h | 1 KB 23FFh-2000h | 512 B 21FFh-2000h |
| Information Memory (FRAM) | Read/Write (Optional Write Protect) ⁽²⁾ | 512B 19FFh-1800h | 512B 19FFh-1800h | 512B 19FFh-1800h |
| Peripherals | Read/Write | 4 KB 0FFFh-0000h | 4 KB 0FFFh-0000h | 4 KB 0FFFh-0000h |

(1) The Program FRAM can be write protected by setting PFWP bit in SYSCFG0 register. Refer to the SYS chapter in the *MSP430FR4xx and MSP430FR2xx Family User's Guide (SLAU445)* for more details

(2) The Information FRAM can be write protected by setting DFWP bit in SYSCFG0 register. Refer to the SYS chapter in the *MSP430FR4xx and MSP430FR2xx Family User's Guide (SLAU445)* for more details

6.11.1 Peripheral File Map

Table 6-29 shows the base address and the memory size of each peripheral's registers, and Table 6-30 through Table 6-49 show all of the available registers for each peripheral and their address offsets.

Table 6-29. Peripherals Summary

| MODULE NAME | BASE ADDRESS | SIZE |
|---------------------------------------|--------------|-------|
| Special Functions (see Table 6-30) | 0100h | 0010h |
| PMM (see Table 6-31) | 0120h | 0020h |
| SYS (see Table 6-32) | 0140h | 0030h |
| CS (see Table 6-33) | 0180h | 0020h |
| FRAM (see Table 6-34) | 01A0h | 0010h |
| CRC (see Table 6-35) | 01C0h | 0008h |
| WDT (see Table 6-36) | 01CCh | 0002h |
| Port P1, P2 (see Table 6-37) | 0200h | 0020h |
| Port P3, P4 (see Table 6-38) | 0220h | 0020h |
| Port P5, P6 (see Table 6-39) | 0240h | 0020h |
| Port P7, P8 (see Table 6-40) | 0260h | 0020h |
| Capacitive Touch I/O (see Table 6-41) | 02E0h | 0010h |
| Timer0_A3 (see Table 6-42) | 0300h | 0030h |
| Timer1_A3 (see Table 6-43) | 0340h | 0030h |
| RTC (see Table 6-44) | 03C0h | 0010h |
| eUSCI_A0 (see Table 6-45) | 0500h | 0020h |
| eUSCI_B0 (see Table 6-46) | 0540h | 0030h |
| LCD (see Table 6-47) | 0600h | 0060h |
| Backup Memory (see Table 6-48) | 0660h | 0020h |
| ADC (see Table 6-49) | 0700h | 0040h |

Table 6-30. Special Function Registers (Base Address: 0100h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-----------------------|----------|--------|
| SFR interrupt enable | SFRIE1 | 00h |
| SFR interrupt flag | SFRIFG1 | 02h |
| SFR reset pin control | SFRRPCR | 04h |

Table 6-31. PMM Registers (Base Address: 0120h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| PMM Control 0 | PMMCTL0 | 00h |
| PMM Control 1 | PMMCTL1 | 02h |
| PMM Control 2 | PMMCTL2 | 04h |
| PMM interrupt flags | PMMIFG | 0Ah |
| PM5 Control 0 | PM5CTL0 | 10h |

Table 6-32. SYS Registers (Base Address: 0140h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-------------------------------------|-----------|--------|
| System control | SYSCTL | 00h |
| Bootstrap loader configuration area | SYSBSLC | 02h |
| JTAG mailbox control | SYSJMBC | 06h |
| JTAG mailbox input 0 | SYSJMBI0 | 08h |
| JTAG mailbox input 1 | SYSJMBI1 | 0Ah |
| JTAG mailbox output 0 | SYSJMBO0 | 0Ch |
| JTAG mailbox output 1 | SYSJMBO1 | 0Eh |
| Bus Error vector generator | SYSBERRIV | 18h |
| User NMI vector generator | SYSUNIV | 1Ah |
| System NMI vector generator | SYSSNIV | 1Ch |
| Reset vector generator | SYSRSTIV | 1Eh |
| System configuration 0 | SYSCFG0 | 20h |
| System configuration 1 | SYSCFG1 | 22h |
| System configuration 2 | SYSCFG2 | 24h |

Table 6-33. CS Registers (Base Address: 0180h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-----------------------|----------|--------|
| CS control register 0 | CSCTL0 | 00h |
| CS control register 1 | CSCTL1 | 02h |
| CS control register 2 | CSCTL2 | 04h |
| CS control register 3 | CSCTL3 | 06h |
| CS control register 4 | CSCTL4 | 08h |
| CS control register 5 | CSCTL5 | 0Ah |
| CS control register 6 | CSCTL6 | 0Ch |
| CS control register 7 | CSCTL7 | 0Eh |
| CS control register 8 | CSCTL8 | 10h |

Table 6-34. FRAM Registers (Base Address: 01A0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| FRAM control 0 | FRCTL0 | 00h |
| General control 0 | GCCTL0 | 04h |
| General control 1 | GCCTL1 | 06h |

Table 6-35. CRC Registers (Base Address: 01C0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-------------------------------|-----------|--------|
| CRC data input | CRC16DI | 00h |
| CRC data input reverse byte | CRCDIRB | 02h |
| CRC initialization and result | CRCINIRES | 04h |
| CRC result reverse byte | CRCRESR | 06h |

Table 6-36. WDT Registers (Base Address: 01CCh)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|------------------------|----------|--------|
| Watchdog timer control | WDTCTL | 00h |

Table 6-37. Port P1, P2 Registers (Base Address: 0200h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|------------------------------------|----------|--------|
| Port P1 input | P1IN | 00h |
| Port P1 output | P1OUT | 02h |
| Port P1 direction | P1DIR | 04h |
| Port P1 pulling register enable | P1REN | 06h |
| Port P1 selection 0 | P1SEL0 | 0Ah |
| Port P1 interrupt vector word | P1IV | 0Eh |
| Port P1 interrupt edge select | P1IES | 18h |
| Port P1 interrupt enable | P1IE | 1Ah |
| Port P1 interrupt flag | P1IFG | 1Ch |
| Port P2 input | P2IN | 01h |
| Port P2 output | P2OUT | 03h |
| Port P2 direction | P2DIR | 05h |
| Port P2 pulling register enable | P2REN | 07h |
| Port P2 selection 0 ⁽¹⁾ | P2SEL0 | 0Bh |
| Port P2 interrupt vector word | P2IV | 1Eh |
| Port P2 interrupt edge select | P2IES | 19h |
| Port P2 interrupt enable | P2IE | 1Bh |
| Port P2 interrupt flag | P2IFG | 1Dh |

(1) Port P2 selection register does not feature any valid bits. P2SEL0 presents for 16-bit Port A operation with P1SEL0.

Table 6-38. Port P3, P4 Registers (Base Address: 0220h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|------------------------------------|----------|--------|
| Port P3 input | P3IN | 00h |
| Port P3 output | P3OUT | 02h |
| Port P3 direction | P3DIR | 04h |
| Port P3 pulling register enable | P3REN | 06h |
| Port P3 selection 0 ⁽¹⁾ | P3SEL0 | 0Ah |
| Port P4 input | P4IN | 01h |
| Port P4 output | P4OUT | 03h |
| Port P4 direction | P4DIR | 05h |
| Port P4 pulling register enable | P4REN | 07h |
| Port P4 selection 0 | P4SEL0 | 0Bh |

(1) Port P3 selection register does not feature any valid bits. P3SEL0 presents for 16-bit Port B operation with P4SEL0.

Table 6-39. Port P5, P6 Registers (Base Address: 0240h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|------------------------------------|----------|--------|
| Port P5 input | P5IN | 00h |
| Port P5 output | P5OUT | 02h |
| Port P5 direction | P5DIR | 04h |
| Port P5 pulling register enable | P5REN | 06h |
| Port P5 selection 0 | P5SEL0 | 0Ah |
| Port P6 input | P6IN | 01h |
| Port P6 output | P6OUT | 03h |
| Port P6 direction | P6DIR | 05h |
| Port P6 pulling register enable | P6REN | 07h |
| Port P6 selection 0 ⁽¹⁾ | P6SEL0 | 0Bh |

(1) Port P6 selection register does not feature any valid bits. P6SEL0 presents for 16-bit Port C operation with P5SEL0.

Table 6-40. Port P7, P8 Registers (Base Address: 0260h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|------------------------------------|----------|--------|
| Port P7 input | P7IN | 00h |
| Port P7 output | P7OUT | 02h |
| Port P7 direction | P7DIR | 04h |
| Port P7 pulling register enable | P7REN | 06h |
| Port P7 selection 0 ⁽¹⁾ | P7SEL0 | 0Ah |
| Port P8 input | P8IN | 01h |
| Port P8 output | P8OUT | 03h |
| Port P8 direction | P8DIR | 05h |
| Port P8 pulling register enable | P8REN | 07h |
| Port P8 selection 0 | P8SEL0 | 0Bh |

(1) Port P7 selection register does not feature any valid bits. P7SEL0 presents for 16-bit Port D operation with P8SEL0.

Table 6-41. Capacitive Touch IO Registers (Base Address: 02E0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-------------------------------|------------|--------|
| Capacitive Touch IO 0 control | CAPTIO0CTL | 0Eh |

Table 6-42. Timer0_A3 Registers (Base Address: 0300h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------------|----------|--------|
| TA0 control | TA0CTL | 00h |
| Capture/compare control 0 | TA0CCTL0 | 02h |
| Capture/compare control 1 | TA0CCTL1 | 04h |
| Capture/compare control 2 | TA0CCTL2 | 06h |
| TA0 counter register | TA0R | 10h |
| Capture/compare register 0 | TA0CCR0 | 12h |
| Capture/compare register 1 | TA0CCR1 | 14h |
| Capture/compare register 2 | TA0CCR2 | 16h |
| TA0 expansion register 0 | TA0EX0 | 20h |
| TA0 interrupt vector | TA0IV | 2Eh |

Table 6-43. Timer1_A3 Registers (Base Address: 0340h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------------|----------|--------|
| TA1 control | TA1CTL | 00h |
| Capture/compare control 0 | TA1CCTL0 | 02h |
| Capture/compare control 1 | TA1CCTL1 | 04h |
| Capture/compare control 2 | TA1CCTL2 | 06h |
| TA1 counter register | TA1R | 10h |
| Capture/compare register 0 | TA1CCR0 | 12h |
| Capture/compare register 1 | TA1CCR1 | 14h |
| Capture/compare register 2 | TA1CCR2 | 16h |
| TA1 expansion register 0 | TA1EX0 | 20h |
| TA1 interrupt vector | TA1IV | 2Eh |

Table 6-44. RTC Registers (Base Address: 03C0h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| RTC control | RTCCTL | 00h |
| RTC interrupt vector | RTCIV | 04h |
| RTC modulo | RTCMOD | 08h |
| RTC counter | RTCCNT | 0Ch |

Table 6-45. eUSCI_A0 Registers (Base Address: 0500h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|-------------------------------|-------------|--------|
| eUSCI_A control word 0 | UCA0CTLW0 | 00h |
| eUSCI_A control word 1 | UCA0CTLW1 | 02h |
| eUSCI_A control rate 0 | UCA0BR0 | 06h |
| eUSCI_A control rate 1 | UCA0BR1 | 07h |
| eUSCI_A modulation control | UCA0MCTLW | 08h |
| eUSCI_A status | UCA0STAT | 0Ah |
| eUSCI_A receive buffer | UCA0RXBUF | 0Ch |
| eUSCI_A transmit buffer | UCA0TXBUF | 0Eh |
| eUSCI_A LIN control | UCA0ABCTL | 10h |
| eUSCI_A IrDA transmit control | IUCA0IRTCTL | 12h |
| eUSCI_A IrDA receive control | IUCA0IRRCTL | 13h |
| eUSCI_A interrupt enable | UCA0IE | 1Ah |
| eUSCI_A interrupt flags | UCA0IFG | 1Ch |
| eUSCI_A interrupt vector word | UCA0IV | 1Eh |

Table 6-46. eUSCI_B0 Registers (Base Address: 0540h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--------------------------------|-------------|--------|
| eUSCI_B control word 0 | UCB0CTLW0 | 00h |
| eUSCI_B control word 1 | UCB0CTLW1 | 02h |
| eUSCI_B bit rate 0 | UCB0BR0 | 06h |
| eUSCI_B bit rate 1 | UCB0BR1 | 07h |
| eUSCI_B status word | UCB0STATW | 08h |
| eUSCI_B byte counter threshold | UCB0TBCNT | 0Ah |
| eUSCI_B receive buffer | UCB0RXBUF | 0Ch |
| eUSCI_B transmit buffer | UCB0TXBUF | 0Eh |
| eUSCI_B I2C own address 0 | UCB0I2COA0 | 14h |
| eUSCI_B I2C own address 1 | UCB0I2COA1 | 16h |
| eUSCI_B I2C own address 2 | UCB0I2COA2 | 18h |
| eUSCI_B I2C own address 3 | UCB0I2COA3 | 1Ah |
| eUSCI_B receive address | UCB0ADDRX | 1Ch |
| eUSCI_B address mask | UCB0ADDMASK | 1Eh |
| eUSCI_B I2C slave address | UCB0I2CSA | 20h |
| eUSCI_B interrupt enable | UCB0IE | 2Ah |
| eUSCI_B interrupt flags | UCB0IFG | 2Ch |
| eUSCI_B interrupt vector word | UCB0IV | 2Eh |

Table 6-47. LCD Registers (Base Address: 0600h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|---|-----------|--------|
| LCD control register 0 | LCDCTL0 | 00h |
| LCD control register 1 | LCDCTL1 | 02h |
| LCD blink control register | LCDBLKCTL | 04h |
| LCD memory control register | LCDMEMCTL | 06h |
| LCD voltage control register | LCDVCTL | 08h |
| LCD port control 0 | LCDPCTL0 | 0Ah |
| LCD port control 1 | LCDPCTL1 | 0Ch |
| LCD port control 2 | LCDPCTL2 | 0Eh |
| LCD COM/SEG select register | LCDCSS0 | 14h |
| LCD COM/SEG select register | LCDCSS1 | 16h |
| LCD COM/SEG select register | LCDCSS2 | 18h |
| LCD interrupt vector | LCDIV | 1Eh |
| Display memory Static and 2 to 4 mux modes | | |
| LCD memory 0 | LCDM0 | 20h |
| LCD memory 1 | LCDM1 | 21h |
| LCD memory 2 | LCDM2 | 22h |
| ⋮ | ⋮ | ⋮ |
| LCD memory 19 | LCDM19 | 33h |
| Reserved ⁽¹⁾ | | 34h |
| ⋮ | ⋮ | ⋮ |
| Reserved ⁽¹⁾ | | 3Fh |

(1) In static and 2-mux to 4-mux modes, LCD memory and blink memory 40 to 63 are not physically implemented.

Table 6-47. LCD Registers (Base Address: 0600h) (continued)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--|----------|--------|
| Blinking memory for Static and 2 to 4 mux modes | | |
| LCD blinking memory 0 | LCDBM0 | 40h |
| LCD blinking memory 1 | LCDBM1 | 41h |
| ⋮ | ⋮ | ⋮ |
| LCD blinking memory 19 | LCDBM19 | 53h |
| Reserved ⁽¹⁾ | | 54h |
| ⋮ | ⋮ | ⋮ |
| Reserved ⁽¹⁾ | | 5Fh |
| Display memory for 5 to 8 mux modes | | |
| LCD memory 0 | LCDM0 | 20h |
| LCD memory 1 | LCDM1 | 21h |
| LCD memory 2 | LCDM2 | 22h |
| ⋮ | ⋮ | ⋮ |
| LCD memory 39 | LCDM39 | 47h |
| Reserved ⁽²⁾ | | 48h |
| ⋮ | ⋮ | ⋮ |
| Reserved ⁽²⁾ | | 5Fh |

(1) In static and 2-mux to 4-mux modes, LCD memory and blink memory 40 to 63 are not physically implemented.

(2) In 5-mux to 8-mux modes, LCD memory and blink memory 40 to 63 are not physically implemented.

Table 6-48. Backup Memory Registers (Base Address: 0660h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|----------------------|----------|--------|
| Backup Memory 0 | BAKMEM0 | 00h |
| Backup Memory 1 | BAKMEM1 | 02h |
| Backup Memory 2 | BAKMEM2 | 04h |
| Backup Memory 3 | BAKMEM3 | 06h |
| Backup Memory 4 | BAKMEM4 | 08h |
| Backup Memory 5 | BAKMEM5 | 0Ah |
| Backup Memory 6 | BAKMEM6 | 0Ch |
| Backup Memory 7 | BAKMEM7 | 0Eh |
| Backup Memory 8 | BAKMEM8 | 10h |
| Backup Memory 9 | BAKMEM9 | 12h |
| Backup Memory 10 | BAKMEM10 | 14h |
| Backup Memory 11 | BAKMEM11 | 16h |
| Backup Memory 12 | BAKMEM12 | 18h |
| Backup Memory 13 | BAKMEM13 | 1Ah |
| Backup Memory 14 | BAKMEM14 | 1Ch |
| Backup Memory 15 | BAKMEM15 | 1Eh |

Table 6-49. ADC Registers (Base Address: 0700h)

| REGISTER DESCRIPTION | REGISTER | OFFSET |
|--------------------------------------|----------|--------|
| ADC control register 0 | ADCCTL0 | 00h |
| ADC control register 1 | ADCCTL1 | 02h |
| ADC control register 2 | ADCCTL2 | 04h |
| ADC window comparator low threshold | ADCLO | 06h |
| ADC window comparator high threshold | ADCHI | 08h |
| ADC memory control register 0 | ADCMCTL0 | 0Ah |
| ADC conversion memory register | ADCMEM0 | 12h |
| ADC interrupt enable | ADCIE | 1Ah |
| ADC interrupt flags | ADCIFG | 1Ch |
| ADC interrupt vector word | ADCIV | 1Eh |

6.12 Identification

6.12.1 Revision Identification

The device revision information is shown as part of the top-side marking on the device package. The device-specific erratasheet describes these markings. For links to all of the erratasheets for the devices in this data sheet, see [Section 8.2](#).

The hardware revision is also stored in the Device Descriptor structure in the Info Block section. For details on this value, see the "Hardware Revision" entries in [Section 6.10](#).

6.12.2 Device Identification

The device type can be identified from the top-side marking on the device package. The device-specific erratasheet describes these markings. For links to all of the erratasheets for the devices in this data sheet, see [Section 8.2](#).

A device identification value is also stored in the Device Descriptor structure in the Info Block section. For details on this value, see the "Device ID" entries in [Section 6.10](#).

6.12.3 JTAG Identification

Programming through the JTAG interface, including reading and identifying the JTAG ID, is described in detail in the *MSP430 Programming Via the JTAG Interface User's Guide* ([SLAU320](#)).

7 Applications, Implementation, and Layout

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

7.1 Device Connection and Layout Fundamentals

This section discusses the recommended guidelines when designing with the MSP430FR413x devices. These guidelines are to make sure that the device has proper connections for powering, programming, debugging, and optimum analog performance.

7.1.1 Power Supply Decoupling and Bulk Capacitors

It is recommended to connect a combination of a 10- μ F plus a 100-nF low-ESR ceramic decoupling capacitor to the DVCC and DVSS pins. Higher-value capacitors may be used but can impact supply rail ramp-up time. Decoupling capacitors must be placed as close as possible to the pins that they decouple (within a few millimeters).

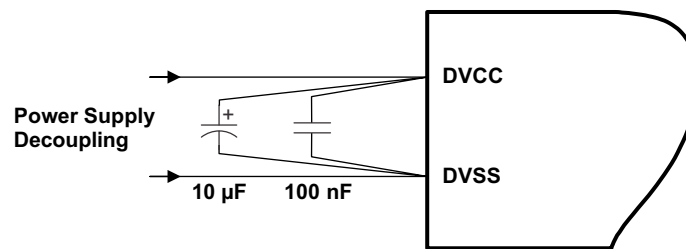


Figure 7-1. Power Supply Decoupling

7.1.2 External Oscillator

This device supports only a low-frequency crystal (32 kHz) on the XIN and XOUT pins. External bypass capacitors for the crystal oscillator pins are required.

It is also possible to apply digital clock signals to the XIN input pin that meet the specifications of the respective oscillator if the appropriate XT1BYPASS mode is selected. In this case, the associated XOUT pin can be used for other purposes. If they are left unused, they must be terminated according to [Section 4.4](#).

Figure 7-2 shows a typical connection diagram.

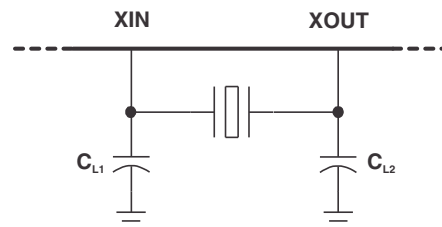


Figure 7-2. Typical Crystal Connection

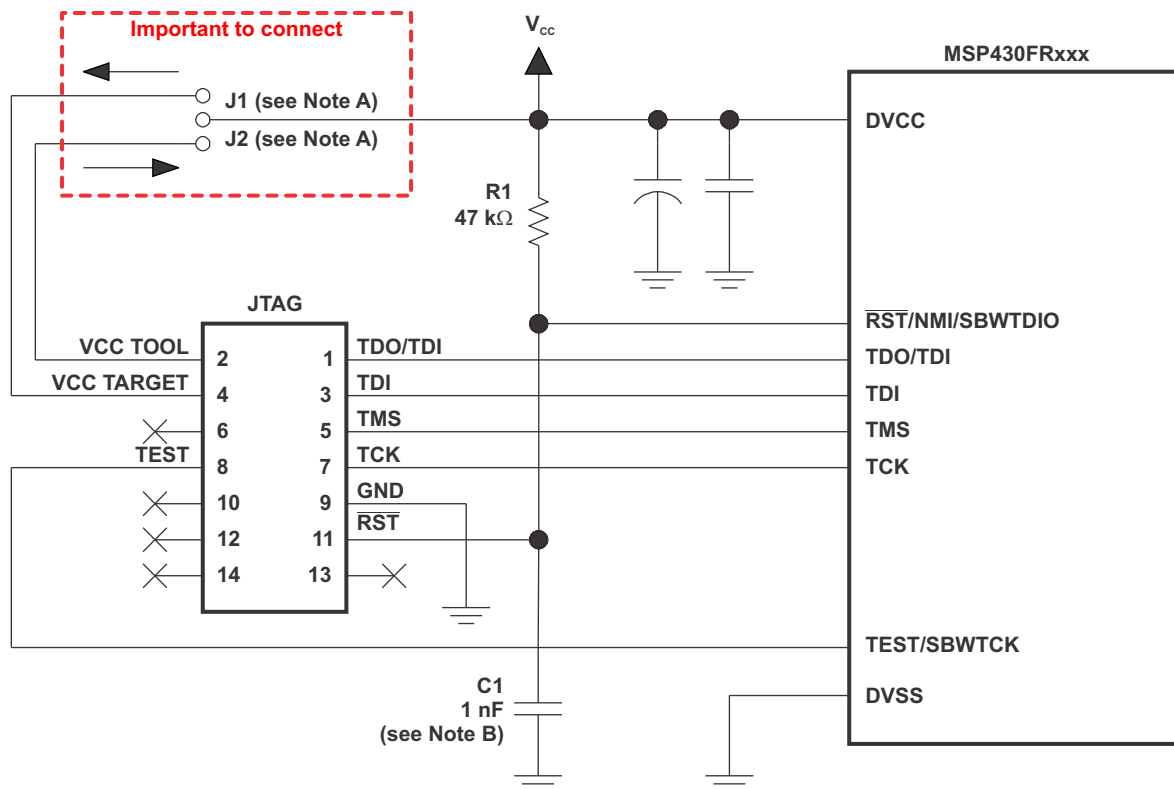
See the application report *MSP430 32-kHz Crystal Oscillators* ([SLAA322](#)) for more information on selecting, testing, and designing a crystal oscillator with the MSP430 devices.

7.1.3 JTAG

With the proper connections, the debugger and a hardware JTAG interface (such as the MSP-FET or MSP-FET430UIF) can be used to program and debug code on the target board. In addition, the connections also support the MSP-GANG production programmers, thus providing an easy way to program prototype boards, if desired. Figure 7-3 shows the connections between the 14-pin JTAG connector and the target device required to support in-system programming and debugging for 4-wire JTAG communication. Figure 7-4 shows the connections for 2-wire JTAG mode (Spy-Bi-Wire).

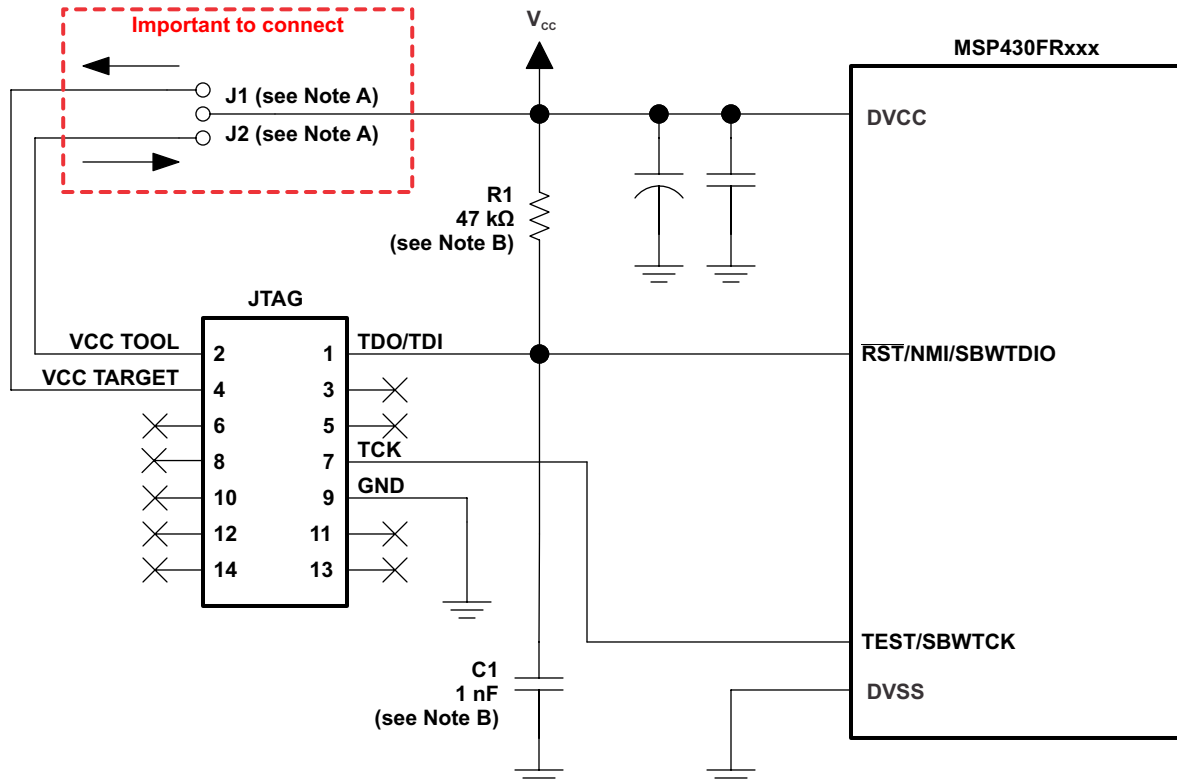
The connections for the MSP-FET and MSP-FET430UIF interface modules and the MSP-GANG are identical. Both can supply VCC to the target board (through pin 2). In addition, the MSP-FET and MSP-FET430UIF interface modules and MSP-GANG have a VCC sense feature that, if used, requires an alternate connection (pin 4 instead of pin 2). The VCC-sense feature senses the local VCC present on the target board (that is, a battery or other local power supply) and adjusts the output signals accordingly. Figure 7-3 and Figure 7-4 show a jumper block that supports both scenarios of supplying VCC to the target board. If this flexibility is not required, the desired VCC connections may be hard-wired to eliminate the jumper block. Pins 2 and 4 must not be connected at the same time.

For additional design information regarding the JTAG interface, see the *MSP430 Hardware Tools User's Guide* (SLAU278).



- A. If a local target power supply is used, make connection J1. If power from the debug or programming adapter is used, make connection J2.
- B. The upper limit for C1 is 1.1 nF when using current TI tools.

Figure 7-3. Signal Connections for 4-Wire JTAG Communication



- Make connection J1 if a local target power supply is used, or make connection J2 if the target is powered from the debug or programming adapter.
- The device $\overline{\text{RST/NMI/SBWTIO}}$ pin is used in 2-wire mode for bidirectional communication with the device during JTAG access, and any capacitance that is attached to this signal may affect the ability to establish a connection with the device. The upper limit for C1 is 1.1 nF when using current TI tools.

Figure 7-4. Signal Connections for 2-Wire JTAG Communication (Spy-Bi-Wire)

7.1.4 Reset

The reset pin can be configured as a reset function (default) or as an NMI function in the Special Function Register (SFR), SFRRPCR.

In reset mode, the $\overline{\text{RST/NMI}}$ pin is active low, and a pulse applied to this pin that meets the reset timing specifications generates a BOR-type device reset.

Setting SYSNMI causes the $\overline{\text{RST/NMI}}$ pin to be configured as an external NMI source. The external NMI is edge sensitive, and its edge is selectable by SYSNMIIES. Setting the NMIIE enables the interrupt of the external NMI. When an external NMI event occurs, the NMIIFG is set.

The $\overline{\text{RST/NMI}}$ pin can have either a pullup or pulldown that is enabled or not. SYSRSTUP selects either pullup or pulldown, and SYSRSTRE causes the pullup (default) or pulldown to be enabled (default) or not. If the $\overline{\text{RST/NMI}}$ pin is unused, it is required either to select and enable the internal pullup or to connect an external 47-k Ω pullup resistor to the $\overline{\text{RST/NMI}}$ pin with a 1.1-nF pulldown capacitor. The pulldown capacitor should not exceed 1.1 nF when using devices with Spy-Bi-Wire interface in Spy-Bi-Wire mode or in 4-wire JTAG mode with TI tools like FET interfaces or GANG programmers.

See the device family user's guide ([SLAU367](#)) for more information on the referenced control registers and bits.

7.1.5 Unused Pins

For details on the connection of unused pins, see [Section 4.4](#).

7.1.6 General Layout Recommendations

- Proper grounding and short traces for external crystal to reduce parasitic capacitance. See the application report *MSP430 32-kHz Crystal Oscillators* ([SLAA322](#)) for recommended layout guidelines.
- Proper bypass capacitors on DVCC and reference pins, if used.
- Avoid routing any high-frequency signal close to an analog signal line. For example, keep digital switching signals such as PWM or JTAG signals away from the oscillator circuit.
- Refer to the *Circuit Board Layout Techniques* design guide ([SLOA089](#)) for a detailed discussion of PCB layout considerations. This document is written primarily about op amps, but the guidelines are generally applicable for all mixed-signal applications.
- Proper ESD level protection should be considered to protect the device from unintended high-voltage electrostatic discharge. See the application report *MSP430 System-Level ESD Considerations* ([SLAA530](#)) for guidelines.

7.1.7 Do's and Don'ts

During power up, power down, and device operation, DVCC must not exceed the limits specified in the [Absolute Maximum Ratings](#) section. Exceeding the specified limits may cause malfunction of the device including erroneous writes to RAM and FRAM.

7.2 Peripheral- and Interface-Specific Design Information

7.2.1 ADC Peripheral

7.2.1.1 Partial Schematic

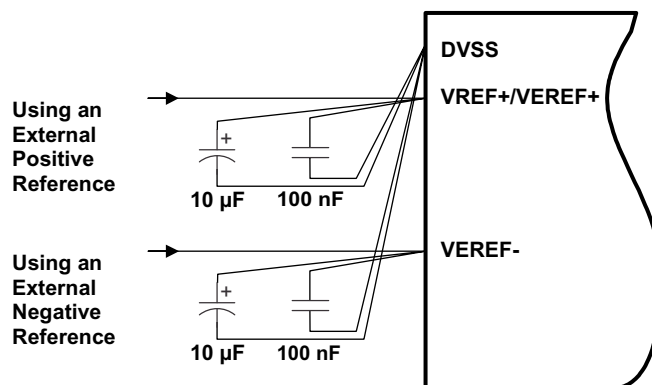


Figure 7-5. ADC Grounding and Noise Considerations

7.2.1.2 Design Requirements

As with any high-resolution ADC, appropriate printed-circuit-board layout and grounding techniques should be followed to eliminate ground loops, unwanted parasitic effects, and noise.

Ground loops are formed when return current from the ADC flows through paths that are common with other analog or digital circuitry. If care is not taken, this current can generate small unwanted offset voltages that can add to or subtract from the reference or input voltages of the ADC. The general guidelines in [Section 7.1.1](#) combined with the connections shown in [Section 7.2.1.1](#) prevent this.

In addition to grounding, ripple and noise spikes on the power-supply lines that are caused by digital switching or switching power supplies can corrupt the conversion result. A noise-free design using separate analog and digital ground planes with a single-point connection is recommended to achieve high accuracy.

Figure 7-5 shows the recommended decoupling circuit when an external voltage reference is used. The internal reference module has a maximum drive current as described in the sections *ADC Pin Enable* and *1.2-V Reference Settings* of the *MSP430FR4xx and MSP430FR2xx Family User's Guide* ([SLAU445](#)).

The reference voltage must be a stable voltage for accurate measurements. The capacitor values that are selected in the general guidelines filter out the high- and low-frequency ripple before the reference voltage enters the device. In this case, the 10- μ F capacitor is used to buffer the reference pin and filter any low-frequency ripple. A bypass capacitor of 100 nF is used to filter out any high-frequency noise.

7.2.1.3 Layout Guidelines

Components that are shown in the partial schematic (see [Figure 7-5](#)) should be placed as close as possible to the respective device pins to avoid long traces, because they add additional parasitic capacitance, inductance, and resistance on the signal.

Avoid routing analog input signals close to a high-frequency pin (for example, a high-frequency PWM), because the high-frequency switching can be coupled into the analog signal.

7.2.2 LCD_E Peripheral

7.2.2.1 Partial Schematic

Required LCD connections greatly vary by the type of display that is used (static or multiplexed), whether external or internal biasing is used, and also whether the on-chip charge pump is employed. For any display used, LCD_E has configurable segment (Sx) or common (COMx) signals connected to the MCU which allows optimal PCB layout and for the design of the application software.

Because LCD connections are application specific, it is difficult to provide a single one-fits-all schematic. However, for an example of connecting a 4-mux LCD with 27 segment lines that has a total of $4 \times 27 = 108$ individually addressable LCD segments to an MSP430FR4133, see the MSP-EXP430FR4133 LaunchPad™ development kit ([MSP-EXP430FR4133](#)) as a reference.

7.2.2.2 Design Requirements

Due to the flexibility of the LCD_E peripheral module to accommodate various segment-based LCDs, selecting the right display for the application in combination with determining specific design requirements is often an iterative process. There can be well-defined requirements in terms of how many individually addressable LCD segments need to be controlled, what the requirements for LCD contrast are, which device pins are available for LCD use and which are required by other application functions, and what the power budget is, to name just a few. TI strongly recommends reviewing the LCD_E peripheral module chapter in the *MSP430FR4xx and MSP430FR2xx Family User's Guide* ([SLAU445](#)) during the initial design requirements and decision process. [Table 7-1](#) provides a brief overview over different choices that can be made and their impact.

Table 7-1. LCD_E Design Options

| OPTION OR FEATURE | IMPACT OR USE CASE |
|--------------------------|---|
| Multiplexed LCD | <ul style="list-style-type: none"> • Enable displays with more segments • Use fewer device pins • LCD contrast decreases as mux level increases • Power consumption increases with mux level • Requires multiple intermediate bias voltages |
| Static LCD | <ul style="list-style-type: none"> • Limited number of segments that can be addressed • Use a relatively large number of device pins • Use the least amount of power • Use only V_{CC} and GND to drive LCD signals |
| Internal Bias Generation | <ul style="list-style-type: none"> • Simpler solution – no external circuitry • Independent of V_{LCD} source • Somewhat higher power consumption |
| External Bias Generation | <ul style="list-style-type: none"> • Requires external resistor ladder divider • Resistor size depends on display • Ability to adjust drive strength to optimize tradeoff between power consumption and good drive of large segments (high capacitive load) • External resistor ladder divider can be stabilized through capacitors to reduce ripple |
| Internal Charge Pump | <ul style="list-style-type: none"> • Helps ensure a constant level of contrast despite decaying supply voltage conditions (battery-powered applications) • Programmable voltage levels allow software-driven contrast control • Requires an external capacitor on the LCDCAP pins • Higher current consumption than simply using V_{CC} for the LCD driver |

7.2.2.3 Detailed Design Procedure

A major component in designing the LCD solution is determining the exact connections between the LCD_E peripheral module and the display itself. Two basic design processes can be employed for this step, although often a balanced co-design approach is recommended:

- PCB layout-driven design
- Software-driven design

In the PCB layout-driven design process, LCD_E offers configurable segment Sx and common COMx signals which are connected to the respective MSP430 device pins so that the routing of the PCB can be optimized to minimize signal crossings and to keep signals on one side of the PCB only, typically the top layer. For example, using a multiplexed LCD, it is possible to arbitrarily connect the Sx and COMx signals between the LCD and the MSP430 device as long as segment lines are swapped with segment lines and common lines are swapped with common lines. It is also possible to not contiguously connect all segment lines but rather skip LCD_E module segment connections to optimize layout or to allow access to other functions that may be multiplexed on a particular device port pin. Employing a purely layout-driven design approach, however, can result in the LCD_E module control bits that are responsible for turning on and off segments to appear scattered throughout the LCD controller's memory map (LCDMx registers). This approach potentially places a rather large burden on the software design that may also result in increased energy consumption due to the computational overhead required to work with the LCD.

The other extreme is a purely software-driven approach that starts with the idea that control bits for LCD segments that are frequently turned on and off together should be co-located in memory in the same LCDMx register or in adjacent registers. For example, in case of a 4-mux display that contains several 7-segment digits, from a software perspective it can be very desirable to control all 7 segments of each digit though a single byte-wide access to an LCDMx register. And consecutive segments are mapped to

consecutive LCDMx registers. This allows use of simple look-up tables or software loops to output numbers on an LCD, reducing computational overhead and optimizing the energy consumption of an application. Establishing of the most convenient memory layout needs to be performed in conjunction with the specific LCD that is being used to understand its design constraints in terms of which segment and which common signals are connected to, for example, a digit.

For design information regarding the LCD controller input voltage selection including internal and external options, contrast control, and bias generation, refer to the LCD_E controller chapter in the *MSP430FR4xx and MSP430FR2xx Family User's Guide* ([SLAU445](#)).

7.2.2.4 Layout Guidelines

LCD segment (Sx) and common (COMx) signal traces are continuously switching while the LCD is enabled and should, therefore, be kept away from sensitive analog signals such as ADC inputs to prevent any noise coupling. TI recommends keeping the LCD signal traces on one side of the PCB grouped together in a bus-like fashion. A ground plane underneath the LCD traces and guard traces employed alongside the LCD traces can provide shielding.

If the internal charge pump of the LCD module is used, the externally provided capacitor on the LCDCAP0 and LCDCAP1 pins should be located as close as possible to the MCU. The capacitor should be connected to the device using a short and direct trace.

For an example layout of connecting a 4-mux LCD with 27 segments to an MSP430FR4133 and using the charge pump feature, see the MSP-EXP430FR4133 LaunchPad development kit ([MSP-EXP430FR4133](#)).

7.3 Typical Applications

[Table 7-2](#) lists several TI Designs reflecting the use of the MSP430FR413x family of devices in different real-world application scenarios. Consult these designs for additional guidance regarding schematic, layout, and software implementation. For the most up to date list of available TI Designs, refer to the device-specific product folders listed in [Section 8.2.1](#).

Table 7-2. TI Designs

| DESIGN NAME | LINK |
|--|---|
| Thermostat Implementation With MSP430FR4xx | TIDM-FRAM-THERMOSTAT |
| Water Meter Implementation With MSP430FR4xx | TIDM-FRAM-WATERMETER |
| Remote Controller of Air Conditioner Using Low-Power Microcontroller | TIDM-REMOTE-CONTROLLER-FOR-AC |

8 Device and Documentation Support

8.1 Device Support

8.1.1 Development Tools Support

8.1.1.1 Hardware Features

See the *Code Composer Studio for MSP430 User's Guide (SLAU157)* for details on the available features.

| MSP430 Architecture | 4-Wire JTAG | 2-Wire JTAG | Break-points (N) | Range Break-points | Clock Control | State Sequencer | Trace Buffer | LPMx.5 Debugging Support |
|---------------------|-------------|-------------|------------------|--------------------|---------------|-----------------|--------------|--------------------------|
| MSP430Xv2 | Yes | Yes | 3 | Yes | Yes | No | No | No |

8.1.1.2 Recommended Hardware Options

All MSP430™ microcontrollers are supported by a wide variety of software and hardware development tools. Tools are available from TI and various third parties. See them all at www.ti.com/msp430tools.

8.1.1.2.1 Target Socket Boards

The target socket boards allow easy programming and debugging of the device using JTAG. They also feature header pin outs for prototyping. Target socket boards are orderable individually or as a kit with the JTAG programmer and debugger included. The following table shows the compatible target boards and the supported packages.

| Package | Target Board and Programmer Bundle | Target Board Only |
|------------------|------------------------------------|--------------------------------|
| 64-pin LQFP (PM) | MSP-FET430U64D | MSP-TS430PM64D |

8.1.1.2.2 Experimenter Boards

Experimenter Boards and Evaluation kits are available for some MSP430 devices. These kits feature additional hardware components and connectivity for full system evaluation and prototyping. See www.ti.com/msp430tools for details.

8.1.1.2.3 Debugging and Programming Tools

Hardware programming and debugging tools are available from TI and from its third party suppliers. See the full list of available tools at www.ti.com/msp430tools.

8.1.1.2.4 Production Programmers

The production programmers expedite loading firmware to devices by programming several devices simultaneously.

| Part Number | PC Port | Features | Provider |
|--------------------------|----------------|---|-------------------|
| MSP-GANG | Serial and USB | Program up to eight devices at a time. Works with PC or standalone. | Texas Instruments |

8.1.1.3 Recommended Software Options

8.1.1.3.1 Integrated Development Environments

Software development tools are available from TI or from third parties. Open source solutions are also available.

This device is supported by Code Composer Studio™ IDE (CCS).

8.1.1.3.2 *MSP430Ware*

[MSP430Ware](#) is a collection of code examples, data sheets, and other design resources for all MSP430 devices delivered in a convenient package. In addition to providing a complete collection of existing MSP430 design resources, MSP430Ware also includes a high-level API called MSP430 Driver Library. This library makes it easy to program MSP430 hardware. MSP430Ware is available as a component of CCS or as a standalone package.

8.1.1.3.3 *Command-Line Programmer*

[MSP430 Flasher](#) is an open-source, shell-based interface for programming MSP430 microcontrollers through a FET programmer or eZ430 using JTAG or Spy-Bi-Wire (SBW) communication. MSP430 Flasher can be used to download binary files (.txt or .hex) files directly to the MSP430 microcontroller without the need for an IDE.

8.1.2 *Device and Development Tool Nomenclature*

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP430 MCU devices and support tools. Each MSP430 MCU commercial family member has one of three prefixes: MSP, PMS, or XMS (for example, MSP430FR4133). Texas Instruments recommends two of three possible prefix designators for its support tools: MSP and MSPX. These prefixes represent evolutionary stages of product development from engineering prototypes (with XMS for devices and MSPX for tools) through fully qualified production devices and tools (with MSP for devices and MSP for tools).

Device development evolutionary flow:

XMS – Experimental device that is not necessarily representative of the final device's electrical specifications

MSP – Fully qualified production device

Support tool development evolutionary flow:

MSPX – Development-support product that has not yet completed Texas Instruments internal qualification testing.

MSP – Fully-qualified development-support product

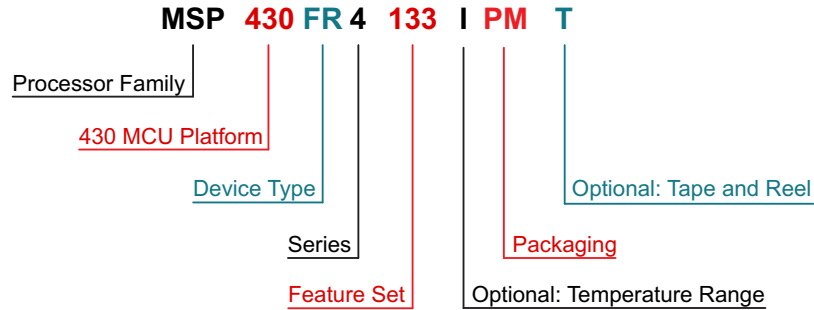
XMS devices and MSPX development-support tools are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

MSP devices and MSP development-support tools have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (XMS) have a greater failure rate than the standard production devices. Texas Instruments recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, PM) and temperature range (for example, T). [Figure 8-1](#) provides a legend for reading the complete device name for any family member.



| | | |
|--------------------------------------|---|---|
| Processor Family | MSP = Mixed Signal Processor XMS = Experimental Silicon | |
| 430 MCU Platform | Ti's 16-bit Low Power Microcontroller Platform | |
| Device Type | Memory Type FR = FRAM | |
| Series | FRAM 4 Series = Up to 16 MHZ + LCD FRAM 2 Series = Up to 16 MHZ without LCD | |
| Feature Set | 1st and 2nd Digit – ADC Channels / 16-bit Timers / I/O 13 = Up to 10 / 3 / Up to 60 | 3rd Digit – FRAM (KB) / SRAM (KB) 3 = 16 / 2 2 = 8 / 1 1 = 4 / 0.5 |
| Optional: Temperature Range | S = 0°C to 50°C I = -40°C to 85°C T = -40°C to 105°C | |
| Packaging | www.ti.com/packaging | |
| Optional: Distribution Format | T = Small Reel R = Large Reel No Marking = Tube or Tray | |

Figure 8-1. Device Nomenclature

8.2 Documentation Support

The following documents describe the MSP430FR413x microcontrollers. Copies of these documents are available on the Internet at www.ti.com.

[SLAU445](#) **MSP430FR4xx and MSP430FR2xx Family User's Guide.** Detailed description of all modules and peripherals available in this device family.

[SLAZ550](#) **MSP430FR4133 Device Erratasheet.** Describes the known exceptions to the functional specifications for all silicon revisions of this device.

[SLAZ551](#) **MSP430FR4132 Device Erratasheet.** Describes the known exceptions to the functional specifications for all silicon revisions of this device.

[SLAZ552](#) **MSP430FR4131 Device Erratasheet.** Describes the known exceptions to the functional specifications for all silicon revisions of this device.

8.2.1 Related Links

Table 8-1 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 8-1. Related Links

| PARTS | PRODUCT FOLDER | SAMPLE & BUY | TECHNICAL DOCUMENTS | TOOLS & SOFTWARE | SUPPORT & COMMUNITY |
|--------------|----------------------------|----------------------------|----------------------------|----------------------------|----------------------------|
| MSP430FR4133 | Click here | Click here | Click here | Click here | Click here |
| MSP430FR4132 | Click here | Click here | Click here | Click here | Click here |
| MSP430FR4131 | Click here | Click here | Click here | Click here | Click here |

8.2.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

[TI E2E™ Community](#)

TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas, and help solve problems with fellow engineers.

[TI Embedded Processors Wiki](#)

Texas Instruments Embedded Processors Wiki. Established to help developers get started with embedded processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

8.3 Trademarks

MSP430, LaunchPad, Code Composer Studio, E2E are trademarks of Texas Instruments. All other trademarks are the property of their respective owners.

8.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

8.5 Glossary

[SLYZ022](#) — *TI Glossary.*

This glossary lists and explains terms, acronyms, and definitions.

9 Mechanical Packaging and Orderable Information

9.1 Packaging Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PRODUCT PREVIEW

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|-------------------|---------------|--------------|--------------------|------|----------------|----------------------------|-------------------------|----------------------|--------------|-------------------------|---------|
| MSP430FR4133IG48R | PREVIEW | TSSOP | DGG | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | FR4133 | |
| MSP430FR4133IG56R | PREVIEW | TSSOP | DGG | 56 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | FR4133 | |
| MSP430FR4133IPMR | PREVIEW | LQFP | PM | 64 | 1000 | TBD | Call TI | Call TI | -40 to 85 | | |
| XMS430FR4133IG48R | ACTIVE | TSSOP | DGG | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | X430FR4133 | Samples |
| XMS430FR4133IG56R | ACTIVE | TSSOP | DGG | 56 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-3-260C-168 HR | -40 to 85 | X430FR4133 | Samples |
| XMS430FR4133IPMR | ACTIVE | LQFP | PM | 64 | 1000 | TBD | Call TI | Call TI | -40 to 85 | | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

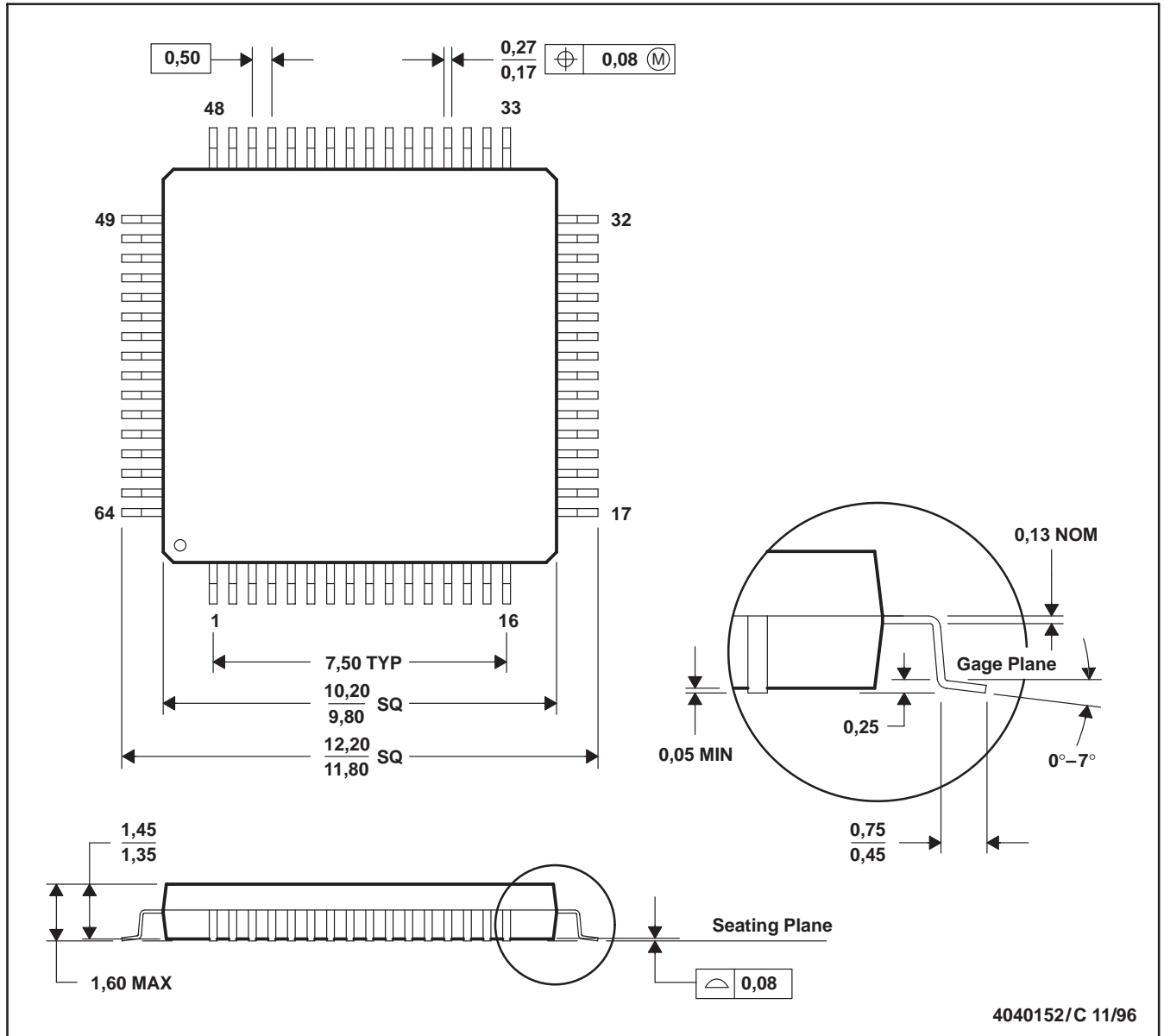
⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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PM (S-PQFP-G64)

PLASTIC QUAD FLATPACK

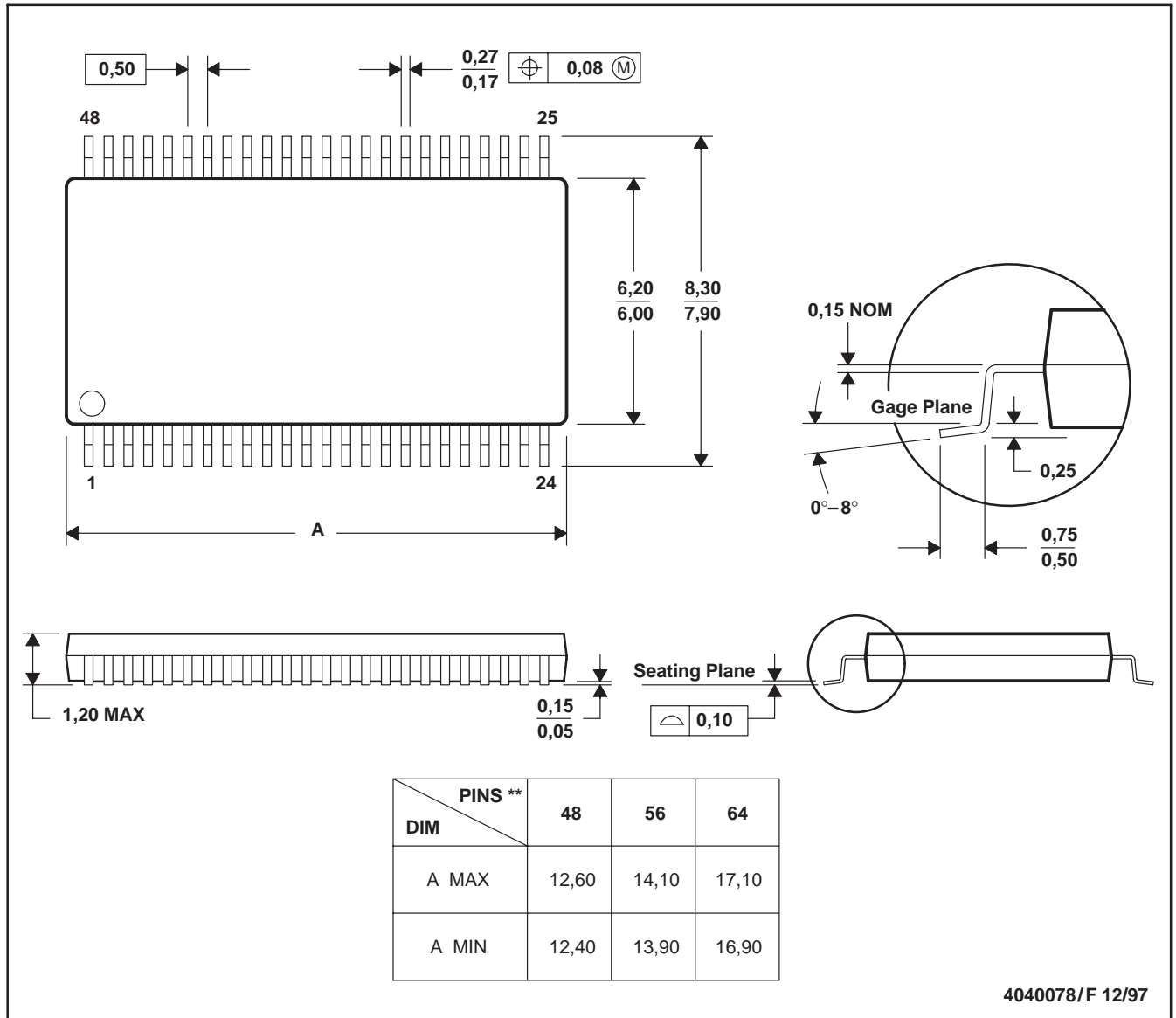


- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Falls within JEDEC MS-026
 D. May also be thermally enhanced plastic with leads connected to the die pads.

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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Products

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| Wireless Connectivity | www.ti.com/wirelessconnectivity |

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